NASA Electronic Parts and Packaging (NEPP) Program - Update of Single Event Upset Field Programmable Gate Array Testing

Melanie Berg, AS&D Inc. in support of the NEPP Program and NASA/GSFC

Melanie.D.Berg@NASA.gov

Kenneth LaBel: NASA/GSFC

Michael Campola: NASA/GSFC

Jonathan Pellish: NASA/GSFC

Acronyms

Acronym	Definition
1MB	1 Megabit
3D	Three Dimensional
3DIC	Three Dimensional Integrated Circuits
ACE	Absolute Contacting Encoder
AHB	Advanced high performance bus
ADC	Analog to Digital Converter
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AF	Air Force
AFRL	Air Force Research Laboratory
AMD	Advanced Micro Devices Incorporated
AMS	Agile Mixed Signal
ARM	Acorn Reduced Instruction Set Computer Machine
AXI	Advanced extensible interface
BAE	British Aerospace
BGA	Ball Grid Array
BOK	Body of Knowledge
BTMR	Block triple modular redundancy
BYU	Brigham Young University
CAN	Controller Area Network
CBRAM	Conductive Bridging Random Access Memory
CCI	Correct Coding Initiative
CGA	Column Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CN	Xilinx ceramic flip-chip (CF and CN) packages are ceramic column grid array (CCGA) packages
COTS	Commercial Off The Shelf
CRC	Cyclic Redundancy Check
CRÈME	Cosmic Ray Effects on Micro Electronics
CRÈME MC	Cosmic Ray Effects on Micro Electronics Monte Carlo
CSE	Crypto Security Engineer
CU	Control Unit
D-Cache	deferred cache
DCU	Distributed Control Unit
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
DFF	Flip-flop
DMM	Digital Multimeter
DMA	Direct Memory Access
DSP	Digital Signal Processing
dSPI	Dynamic Signal Processing Instrument
DTMR	Distributed triple modular redundancy
Dual Ch.	Dual Channel
DUT	Device under test
ECC	Error-Correcting Code
EDAC	Error detection and correction
EEE	Electrical, Electronic, and Electromechanical
EMAC	Equipment Monitor And Control
EMIB	Multi-die Interconnect Bridge
EPCS	Extended physical coding layer
ESA	European Space Agency
eTimers	Event Timers
ETW	Electronics Technology Workshop
FCCU	Fluidized Catalytic Cracking Unit
FeRAM	Ferroelectric Random Access Memory
FinFET	Fin Field Effect Transistor
FIR	Finite impulse response filter
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
FY	Fiscal Year
Gb	Gigabit
Gbps	Gigabit per second
GCR	Galactic Cosmic Ray
GEO	geostationary equatorial orbit
GIC	Global Industry Classification
GOMACTech	Government Microcircuit Applications and Critical Technology Conference
GPIO	General purpose input/output
GPIB	General purpose interface bus
GPU	Graphics Processing Unit
GRC	NASA Glenn Research Center
GSFC	Goddard Space Flight Center

Acronym	Definition
GSN	Goal Structured Notation
GTH/GTY	Transceiver Type
GTMR	Global TMR
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Test
HBM	High Bandwidth Memory
HDIO	High Density Digital Input/Output
HDR	High-Dynamic-Range
HiREV	High Reliability Virtual Electronics Center
HMC	Hybrid Memory Cube
HOST	Hardware Oriented Security and Trust
HP Labs	Hewlett-Packard Laboratories
HPIO	High Performance Input/Output
HPS	High Pressure Sodium
HSTL	High speed transceiver logic
I/F	interface
I/O	input/output
I2C	Inter-Integrated Circuit
i2MOS	Microsemi second generation of Rad-Hard MOSFET
IC	Integrated Circuit
I-Cache	independent cache
JFAC	Joint Federated Assurance Center
JPEG	Joint Photographic Experts Group
JPL	Jet propulsion laboratory
JTAG	Joint Test Action Group (FPGAs use JTAG to provide access to their programming debug/emulation functions)
KB	Kilobyte
L2 Cache	independent caches organized as a hierarchy (L1, L2, etc.)
LCDT	NEPP low cost digital tester
LEO	Low Earth Orbit
LET	Linear energy transfer
L-mem	Long-Memory
LANL	Los Alamos National Laboratory
LP	Low Power
LUT	Look-up table
LVCMOS	Low-voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low –voltage transistor-transistor logic
LTMR	Local triple modular redundancy
LW HPS	Lightwatt High Pressure Sodium
M/L BIST	Memory/Logic Built-In Self-Test
Mil-STD	Military standard
MAPLD	Military Aerospace Programmable Logic Device
MBMA	Model-Based Missions Assurance
MFTF	Mean fluence to failure
µPROM	Micro programmable read-only memory
µSRAM	Micro SRAM
Mil/Aero	Military/Aerospace
MIPI	Mobile Industry Processor Interface
MMC	MultiMediaCard
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MP	Microprocessor
MP	Multiport
MPFE	Multiport Front-End
MPSoC	Multiprocessor System on a chip
MPU	Microprocessor Unit
Msg	message
MTTF	Mean time to failure
NAND	Negated AND or NOT AND
NASA	National Aeronautics and Space Administration
NASA STMD	NASA's Space Technology Mission Directorate
Navy Crane	Naval Surface Warfare Center, Crane, Indiana
NEPP	NASA Electronic Parts and Packaging
NGSP	Next Generation Space Processor
NOR	Not OR logic gate

Acronym	Definition
NRL	Naval Research Laboratory
NRO	National Reconnaissance Office
OCM	On-chip RAM
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCIe Gen2	Peripheral Component Interconnect Express Generation 2
Pconfiguration	SEU cross-section of configuration
Pfunctional_logic	SEU cross-section of functional logic
PHY	Physical layer
PLL	Phase Locked Loop
PMA	Physical Medium Attachment
POR	Power on reset
Proc.	Processing
PS-GTR	High Speed Bus Interface
PSEFI	SEU cross-section from single event functional interrupts
Psystem	System SEU cross-section
QDR	quad data rate
QFN	Quad Flat Pack No Lead
QML	Qualified manufactures list
QSPI	Serial Quad Input/Output
RADECS	IEEE Radiation and its Effects on Components and Systems
RC	Resistor capacitor
R&M	Reliability and Maintainability
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
RGB	Red, Green, and Blue
RH	Radiation Hardened
RT	Radiation Tolerant
SATA	Serial Advanced Technology Attachment
SCU	Secondary Control Unit
SD	Secure Digital
SD/eMMC	Secure Digital embedded MultiMediaCard
SD-HC	Secure Digital High Capacity
SDM	Spatial-Division-Multiplexing
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single event latchup
SERDES	Serializer/deserializer
SET	Single event transient
SEU	Single event upset
Si	Silicon
SK Hynix	SK Hynix Semiconductor Company
SMDs	Selected Item Descriptions
SMMU	System Memory Management Unit
SNL	Sandia National Laboratories
SOA	Safe Operating Area
SOC	Systems on a Chip
SPI	Serial Peripheral Interface
SSTL	Sub series terminated logic
TBD	To Be Determined
Temp	Temperature
THD+N	Total Harmonic Distortion Plus Noise
TMR	Triple Modular Redundancy
T-Sensor	Temperature-Sensor
TSMC	Taiwan Semiconductor Manufacturing Company
UART	Universal Asynchronous Receiver/Transmitter
UltraRAM	Ultra Random Access Memory
USB	Universal Serial Bus
VNAND	Vertical NAND
WDT	Watchdog Timer
WSR	Windowed shift register
XAUI	Extended 10 Gigabit Media Independent Interface
XGXS	10 Gigabit Ethernet Extended Sublayer
XGMII	10 Gigabit Media Independent Interface)
XWSG	Xilinx Security Working Group

Outline

- Field programmable gate array (FPGA) test guidelines.
- Microsemi RTG4 heavy-ion results.
- Xilinx Kintex-UltraScale heavy-ion results.
- Xilinx UltraScale+ single event effect (SEE) test plans.
- Development of a new methodology for characterizing single event upset (SEU) system response.
- NEPP involvement with FPGA security and trust.

NEPP – Processors, Systems on a Chip (SOC), and Field Programmable Gate Arrays (FPGAs)

State of the Art COTS Processors
- Sub 32nm CMOS, FinFETs, etc
- Samsung, Intel, AMD

"Space" FPGAs
- Microsemi RTG4
- Xilinx MPSOC+
- ESA Brave (future)
- "Trusted" FPGA (future)

Graphics Processor Units (GPUs)
- Intel, AMD, Nvidia
- Enabling data processing

COTS FPGAs
- Xilinx Kintex+
- Mitigation evaluation
- TBD: Microsemi PolarFire

Radiation Hardened Processor Evaluation
- BAE
- Vorago (microcontrollers)

Best Practices and Guidelines

Partnering
- Processors: Navy Crane, BAE/NRO-
- FPGAs: AF, Aerospace, SNL, LANL, BYU,…
- Microsemi, Xilinx, Synopsis
- Cubic Aerospace

Potential future task areas:

artificial intelligence (AI) hardware, Intel Stratix 10

FPGA SEU Test Guidelines

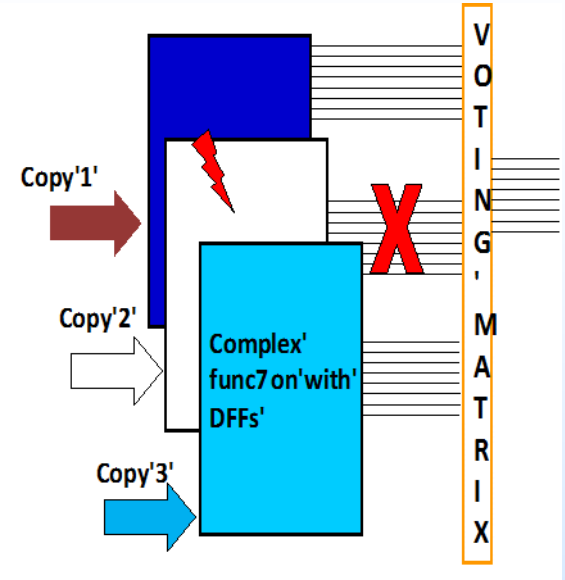
- **Impact to community:**
  - **It is challenging to compare device under test (DUT) SEU data because of differences in test vehicle and test methodology.**
  - **The FPGA SEU Test Guidelines Document creates standardized test methodologies and provide a means for data comparison across organizations and FPGA types.**
  - **The FPGA SEU Test Guidelines Document points out best practices for DUT test structures, monitoring DUT functional response, visibility in DUT operation, DUT control, and DUT power.**
- **Update of the test guideline best practices will be available by December 2017.**
  - **Additional test structures for SEU investigations.**
  - **Additional "do's" and "should-not-do's."**
  - **Embedded processor testing techniques.**

https://nepp.nasa.gov/files/23779/fpga_radiation_test_guidelines_2012.pdf

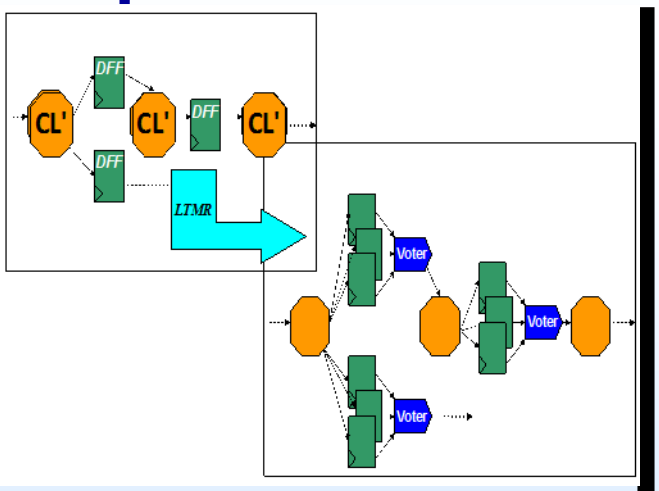
NEPP FPGA Radiation Testing

- NEPP rarely uses evaluation boards for FPGA testing.
  - But when we do… Evaluation boards are generally used for quick-to-beam or flush out testing.
- Low cost digital tester (LCDT) – board with FPGA that supplies DUT stimulus and monitors DUT response.
- Custom built DUT board that connects via high speed interface to the LCDT.
- Visibility of DUT response is significantly enhanced versus evaluation boards.
- LCDT is state machine based (not processor based). Provides fine grained monitoring and reporting (*ns* versus *s*).
  - Hak Kim and the NEPP engineering team built the LCDT board.
  - Custom test controls are designed into the LCDT FPGA.
  - Custom test structures are designed into the DUT FPGA.

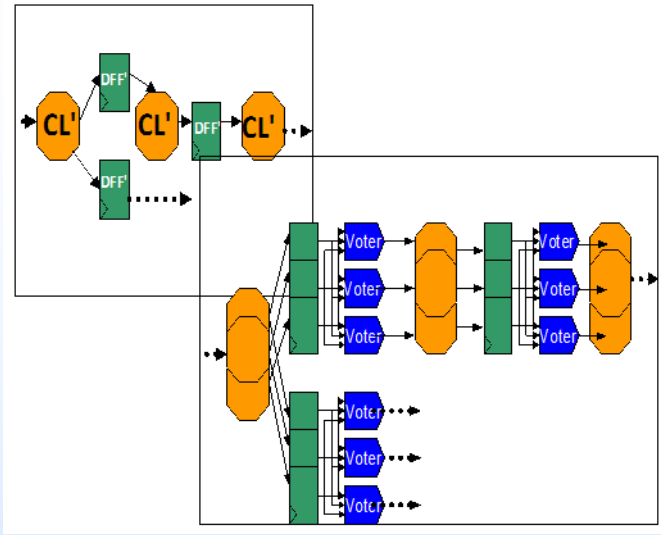
Various Triple Modular Redundant (TMR) Schemes Implemented in FPGA Devices



Block diagram of block TMR (BTMR): a complex function containing combinatorial logic (CL) and flip-flops (DFFs) is triplicated as three black boxes; majority voters are placed at the outputs of the triplet.



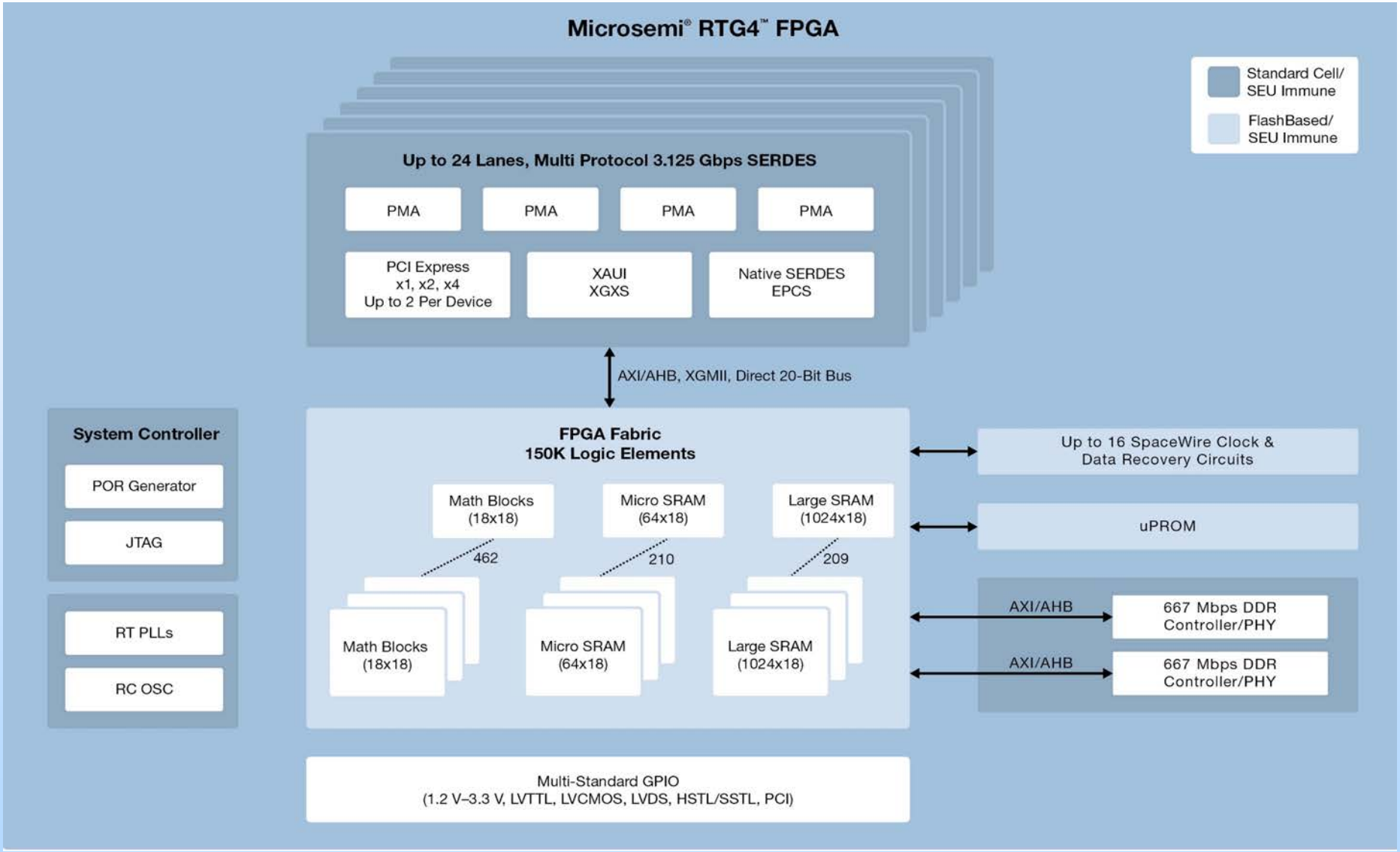
Block diagram of local TMR (LTMR): only flip-flops (DFFs) are triplicated and data-paths stay singular; voters are brought into the design and placed in front of the DFFs.



Block Diagram of distributed TMR (DTMR): the entire design is triplicated except for the global routes (e.g., clocks); voters are brought into the design and placed after the flip-flops (DFFs). DTMR masks and corrects most single event upsets (SEUs).

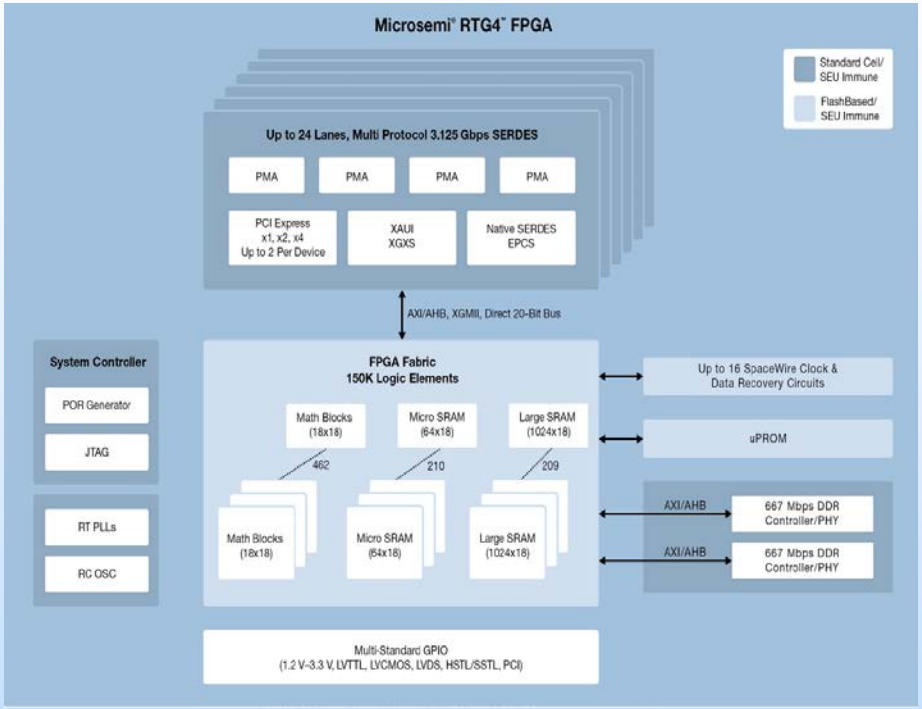
TMR can be embedded in the FPGA or user inserted.

FPGA Devices Manufactured as Space-Grade Products: Microsemi RTG4 FPGA



Impact to Community Microsemi RTG4 FPGA

- Next generation of the space-grade Microsemi RTAXs family.
- I/O interfaces are significantly more robust versus prior Microsemi space-grade FPGAs devices.
- Embedded mitigation, packaging, and qualification process makes this device space-grade.
- Flash based configuration – hence configuration is essentially SEU immune.
- Embedded flip-flop (DFF) SEU hardening.



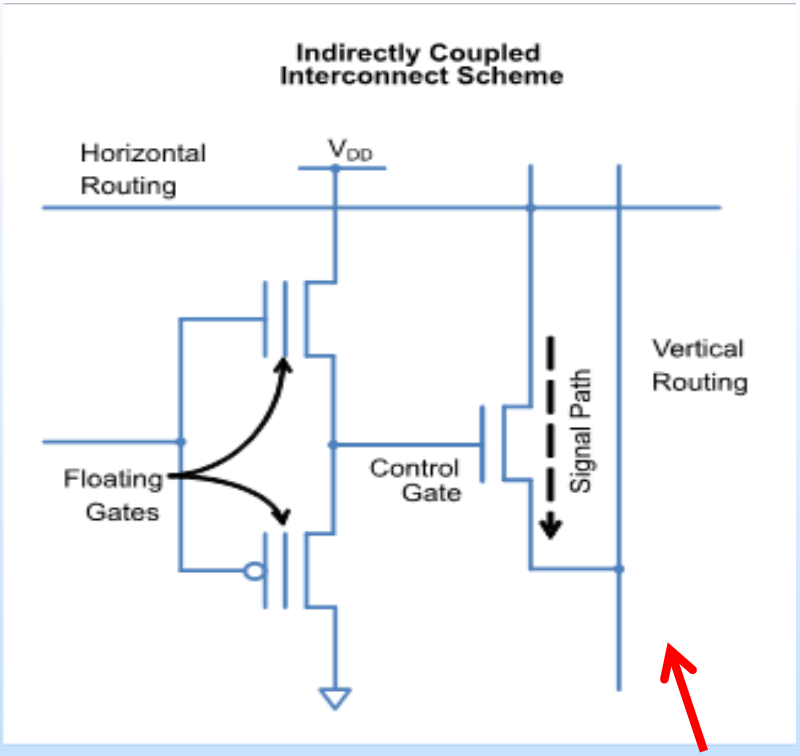
NEPP performs an independent study to determine the level of SEU susceptibility for the various RTG4 components.

Microsemi RTG4: Device Under Test (DUT) Details

- **New Entry into the Aerospace Market with Space-grade Expectation.**
  - **Bulk UMC 65nm CMOS process with an epitaxial layer. Flash based configuration.**
  - **Qualified to MIL-STD-883 Class B, and Microsemi will seek QML Class Q and Class V qualification.**
- **The DUT : RT4G150-CG1657M.**
- **We tested Rev B and Rev C devices.**
- **The DUT contains;**
  - ***158214 look up tables (4-input LUTs);***
  - ***158214 flip-flops (DFFs); 720 user I/O;***
  - ***210K Micro-SRAM (uSRAM) bits;***
  - ***209 18Kblocks of Large-SRAM (LSRAM);***
  - ***462 Math logic blocks (DSP Blocks);***
  - ***8 PLLs; and 48 global routes (radiation-hardened global routes);***

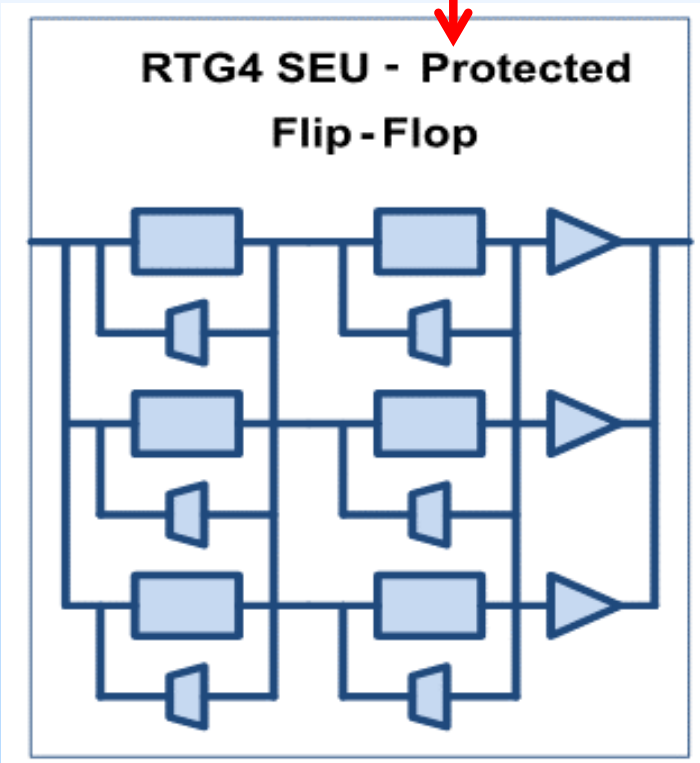
LUT: look up table.
SRAM: sequential random access memory.
DSP: digital signal processing.
PLL: phase locked loop.

Microsemi RTG4: Device Under Test (DUT) Embedded Hardening



Hardened configuration flash cell

DFFs are radiation hardened using LTMR and SET filters placed at the DFF data input.



Microsemi RTG4 Study Objectives

- This is an independent investigation that evaluates the single event destructive and transient susceptibility of the Microsemi RTG4 device.
- Design/Device susceptibility is determined by monitoring the DUT for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing the DUT to a heavy ion beam.
- Potential Single Event Latch-up (SEL) is checked throughout heavy-ion testing by monitoring device current.
- The objectives of this study are the following:
  - Analyze flip-flop (DFF) + combinatorial logic (CL) behavior in simple designs such as shift registers. Compare SEU behavior to more complex designs such as counters and finite impulse response (FIR) filters. Evaluating data trends helps in extrapolating test data to actual designs.
  - Analyze global route behavior – clocks, resets.
  - Analyze configuration susceptibility.

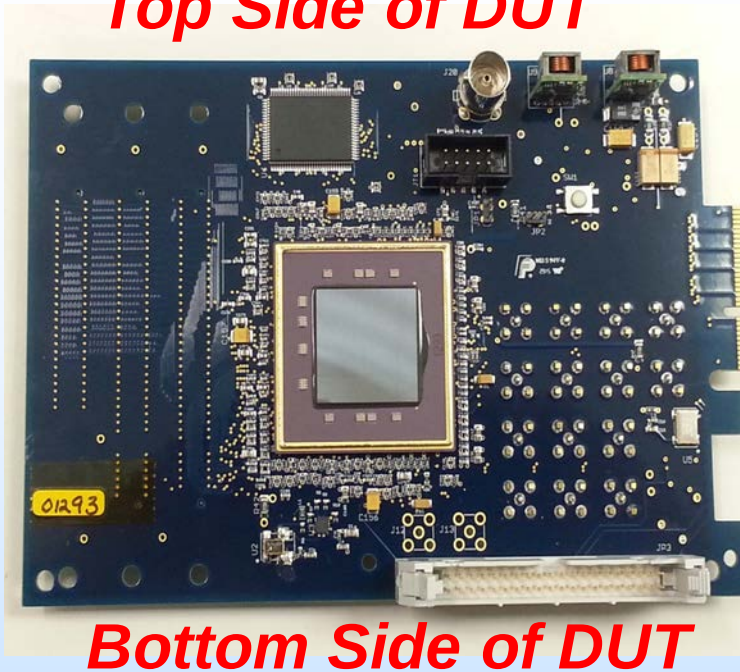
$$P(fs)_{system} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Design σ_{SEU} Configuration σ_{SEU} Functional logic σ_{SEU} SEFI σ_{SEU}

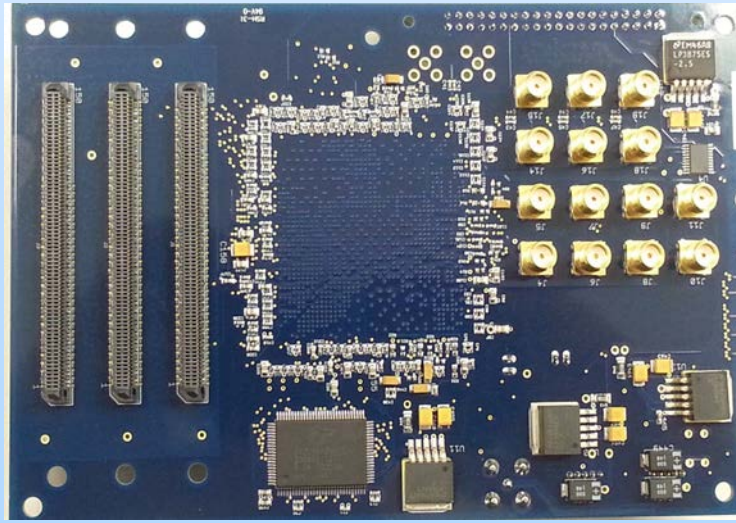
DUT Preparation

- NEPP has populated two Rev B and four populated Rev C boards with RT4G150-CG1657M devices.
- The parts (DUTs) were thinned using mechanical etching via an Ultra Tec ASAP-1 device preparation system.
- The parts have been successfully thinned to 70um – 90um.

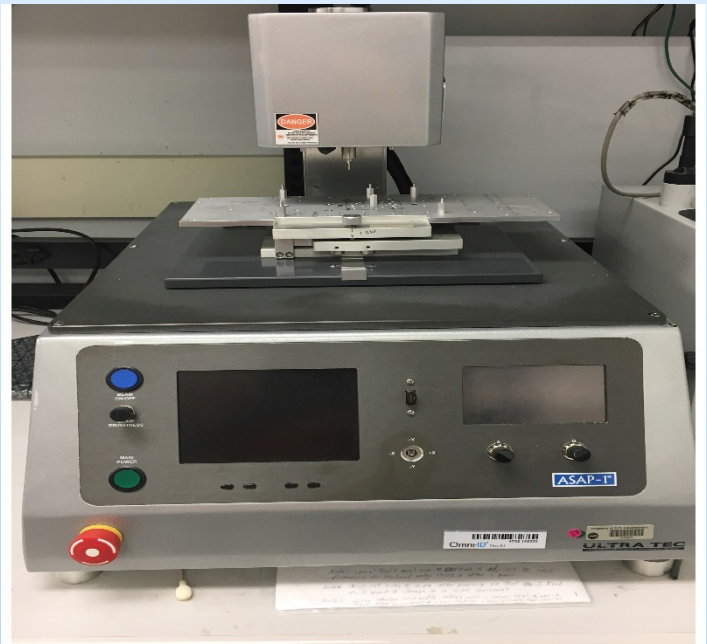
Top Side of DUT



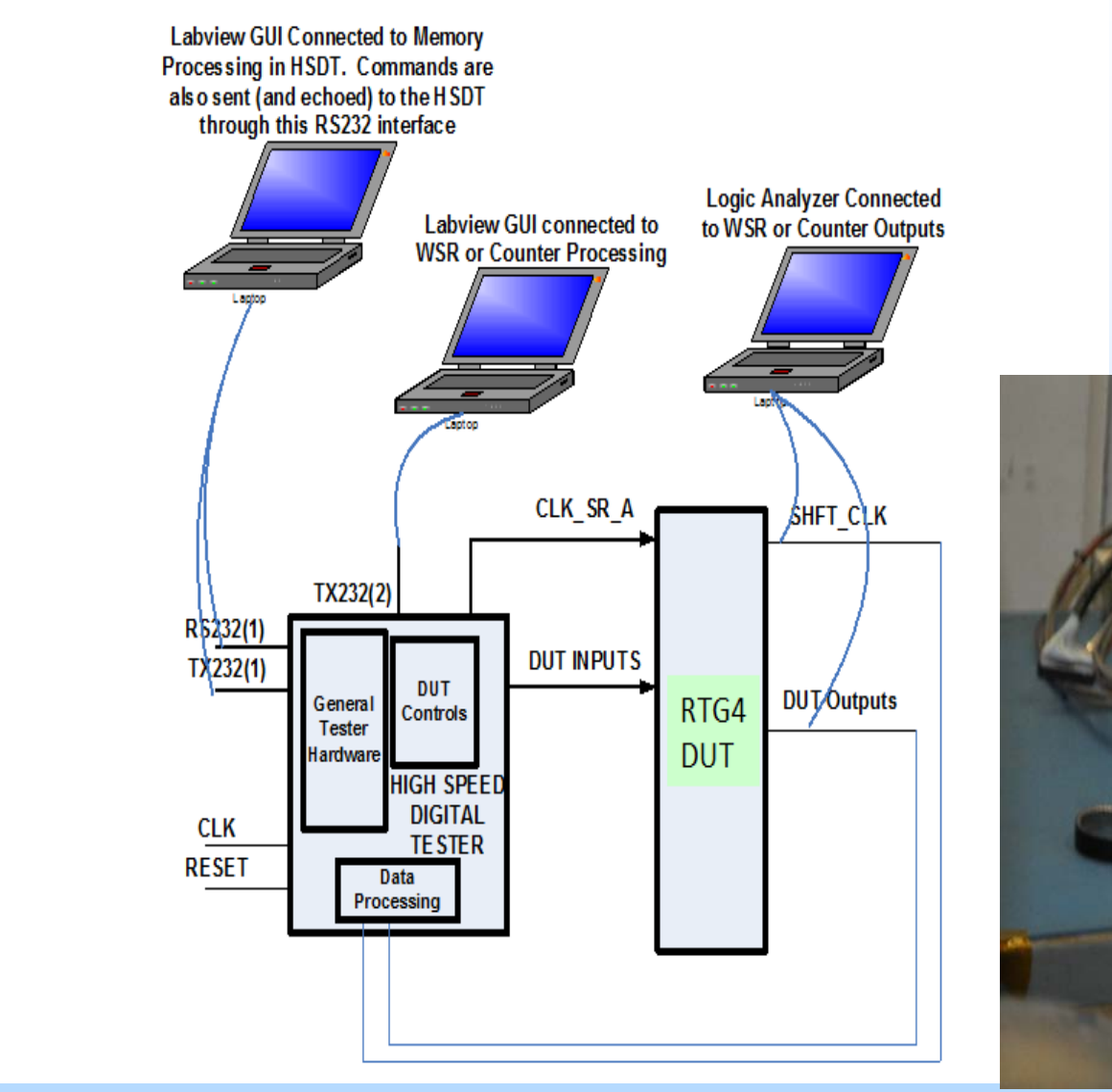
Bottom Side of DUT

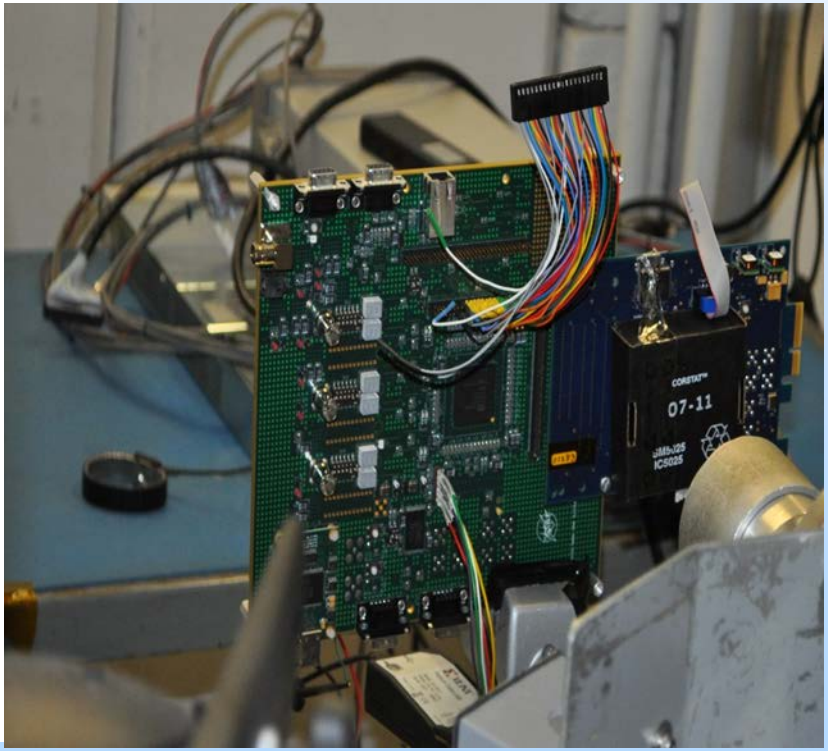


Ultra Tec ASAP-1



Test Setup


Labview GUI Connected to Memory Processing in HSDT. Commands are also sent (and echoed) to the HSDT through this RS232 interface
Labview GUI connected to WSR or Counter Processing
Logic Analyzer Connected to WSR or Counter Outputs
CLK_SR_A
SHFT_CLK
TX232(2)
RS232(1)
TX232(1)
General Tester Hardware
DUT Controls
DUT INPUTS
RTG4 DUT
DUT Outputs
HIGH SPEED DIGITAL TESTER
CLK
RESET
Data Processing



Challenges for Testing

TID: total ionizing dose

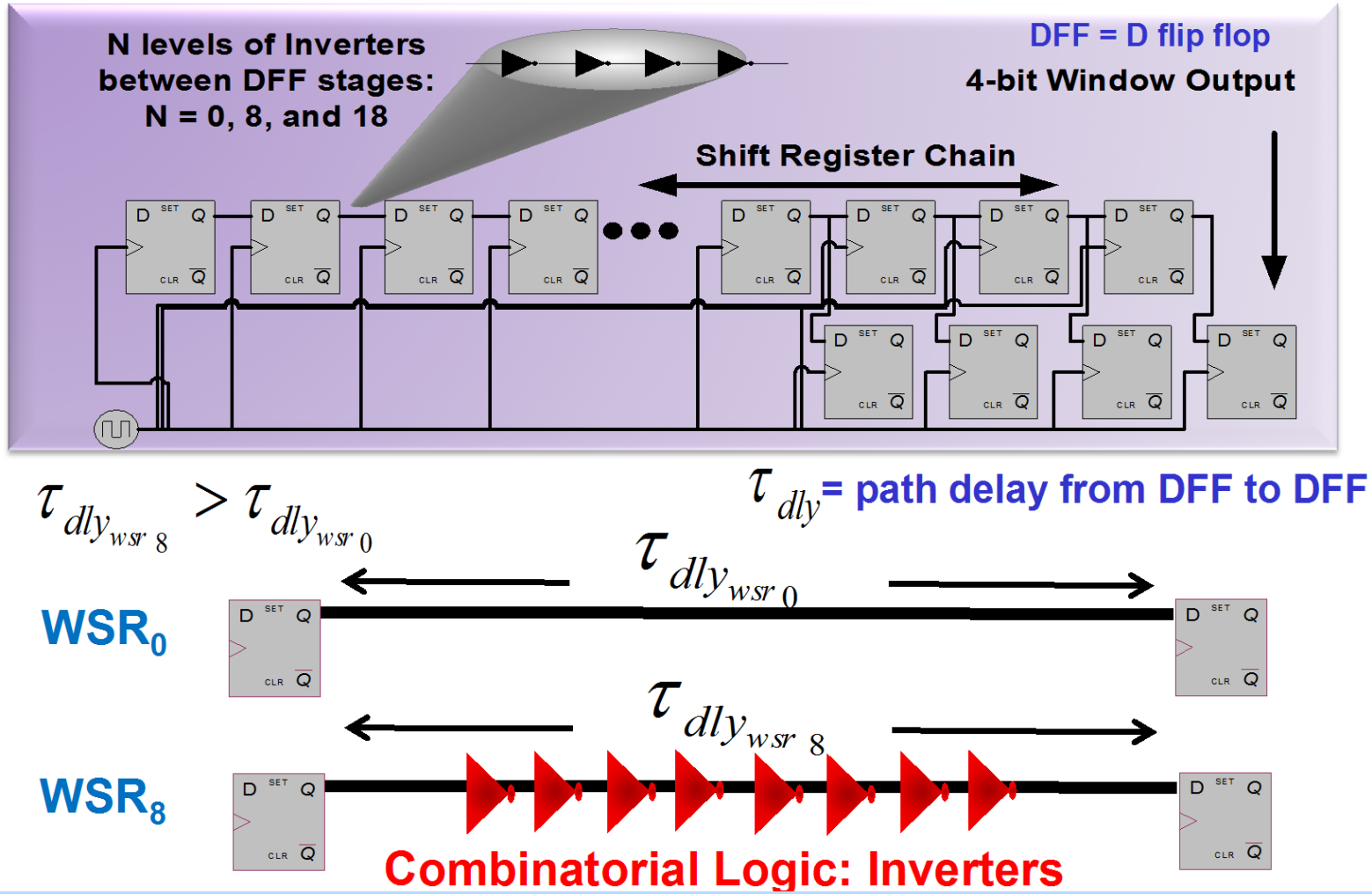
- **Software is new… place and route is not optimal yet. Hence, it is difficult to get high speed without manual placement.**
- **Microsemi reports that devices show TID tolerance up to 160Krads.**
  - **When testing with heavy-ions, dose tolerance will be much higher.**
  - **TID limits the amount of testing per device.**
  - **Number of devices are expensive and are limited for radiation testing.**
  - **A large number of tests are required.**
- **We will always need more parts and beam time.**
- **Current consortium participants:**
  - **NEPP (Goddard and JPL),**
  - **Aerospace Corporation, and**
  - **Microsemi.**

Microsemi RTG4 Designs Tested

Test Structure	Frequency Range
Global routes	2KHz – 150MHz
Shift Registers (WSRs)	2KHz – 150MHz
Counters	5MHz – 100MHz
Finite impulse response filters (FIRs). Math-block (DSP) testing	1MHz-100MHz
Embedded SRAM	N/A

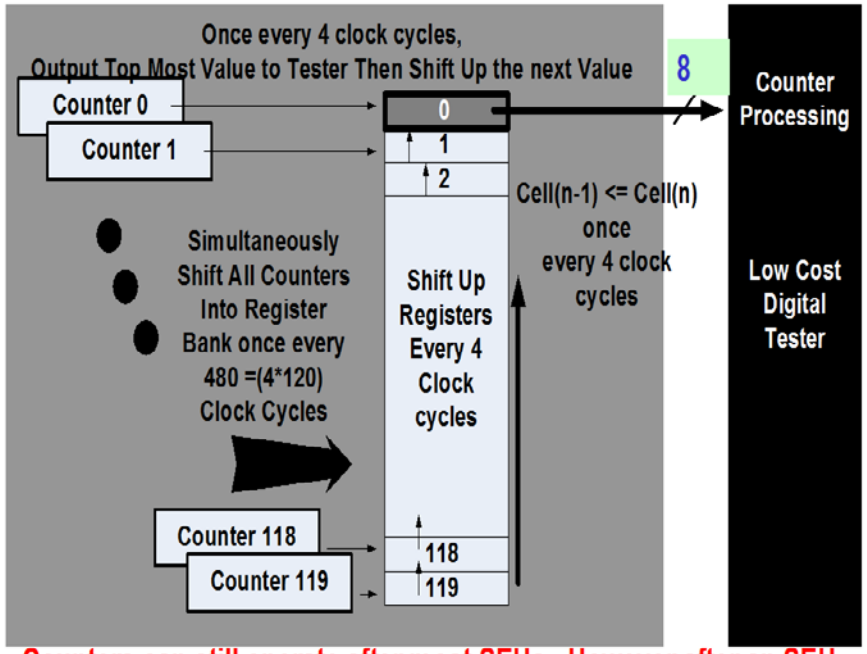
Test structures selected in order to investigate specific RTG4 components and data trends across a variety of designs.

Windowed Shift Registers (WSRs): Test Structure



Counter Arrays

- DUT contains two sets of the following:
  - 200 8-bit counters
  - 200 8-bit snapshot registers
- All counters and snapshot registers are connected to the same clock tree and RESET.
- The clock tree is fed by the clock (CLK) input from the LCDT.
- DUT CLK is connected to a dedicated clock input pin and a clock buffer (CLKBUF used for clock distribution).
- The LCDT sends a clock and a reset to the DUT. The controls are set by the user



Counters can still operate after most SEUs. However after an SEU occurs, the tester must recalculate a new expected value for the affected counter.

2 sets of counter arrays are tested simultaneously

Test Facility Conditions: Texas A&M University Cyclotron Facility

- 25 MeV/amu tune.
- Flux: 1 x 10^4 to 5 x 10^5 particles/cm^2·s
- Fluence: All tests were run to 1 x 10^7 particles/cm^2 or until destructive or functional events occurred.
- Test temperature: Room temperature

Ion	Energy (MEV/Nucleon)	LET (MeV*cm^2/mg) 0°	LET (MeV*cm^2/mg) 60 °
He	25	.07	.14
N	25	.9	1.8
Ne	25	1.8	3.6
Ar	25	5.5	11.0
Kr	25	19.8	40.0
Xe**	25	38.9	78.8

We were unable to obtain Xe during our testing

Test Facility Conditions: Lawrence Berkeley National Laboratory Cyclotron Facility

- 16 MeV/amu tune.
- Flux: 1 x 10^4 to 5 x 10^5 particles/cm^2·s
- Fluence: All tests were run to 1 x 10^7 particles/cm^2 or until destructive or functional events occurred.
- Test temperature: Room temperature

Ion	Energy (MEV/Nucleon)	LET (MeV*cm^2/mg) 0°
N	16	1.16
Ne	16	2.39
Si	16	4.35
Ar	16	7.27
V	16	10.9
Cu	16	16.5
Kr	16	25
Xe	16	49.3

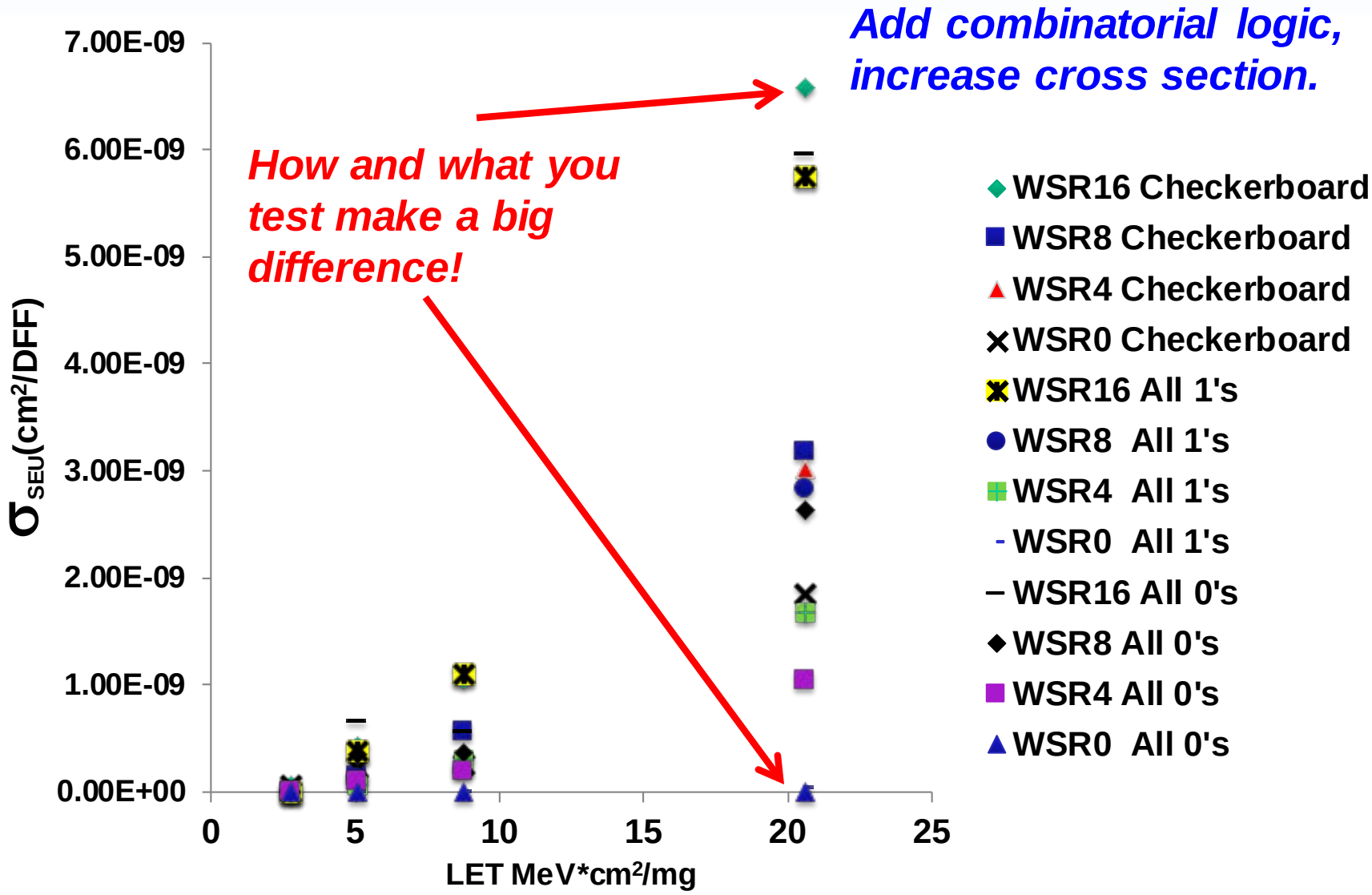
Heavy-Ion Configuration Re-programmability Results

- Re-programmability requires three steps: erase, write, and verify.
- Re-programmability duration is in the order of minutes.
- During this test campaign, tests were only performed up to an LET of 49.3MeVcm^2/mg.
- Higher LETs will be used during future testing.
- No re-programmability failures were observed up to an LET of 49.3MeVcm^2/mg when within particle dose limits. We did not try to reprogram while the beam was turned on.
- Our test methodology is different than Microsemi. They tested re-programmability during exposure to an accelerated particle flux. Programmability failures occurred because of the duration of programmability time versus particle flux.

Heavy-ion Global Route Results

- **Global routes are the backbone of all designs. Hence, it is imperative to investigate global route SEU susceptibility.**
- **For NEPP DUT test structures, clock trees were connected to a variety of sources:**
  - **Direct clock I/O (clock is generated off-chip),**
  - **Internal Oscillator (clock is generated ON-chip),**
  - **Clock conditioning circuit (PLL) (clock is generated off-chip)**
  - **TMR clock conditioning circuit (TMR PLL) (clock is generated off-chip).**
- **Summary of global route results starting from best performance:**
  - **Direct clock I/O had the lowest SEU susceptibility (best performance.**
  - **Clock conditioning circuit had higher SEU susceptibility than direct clock I/O. However, performance can still be acceptable for critical missions.**
  - **TMR clock conditioning circuit (TMR PLL) did not appear to reduce susceptibility and might have higher susceptibility at higher frequencies.**
  - **Internal oscillator clock is SEU soft and should not be used in critical circuits.**

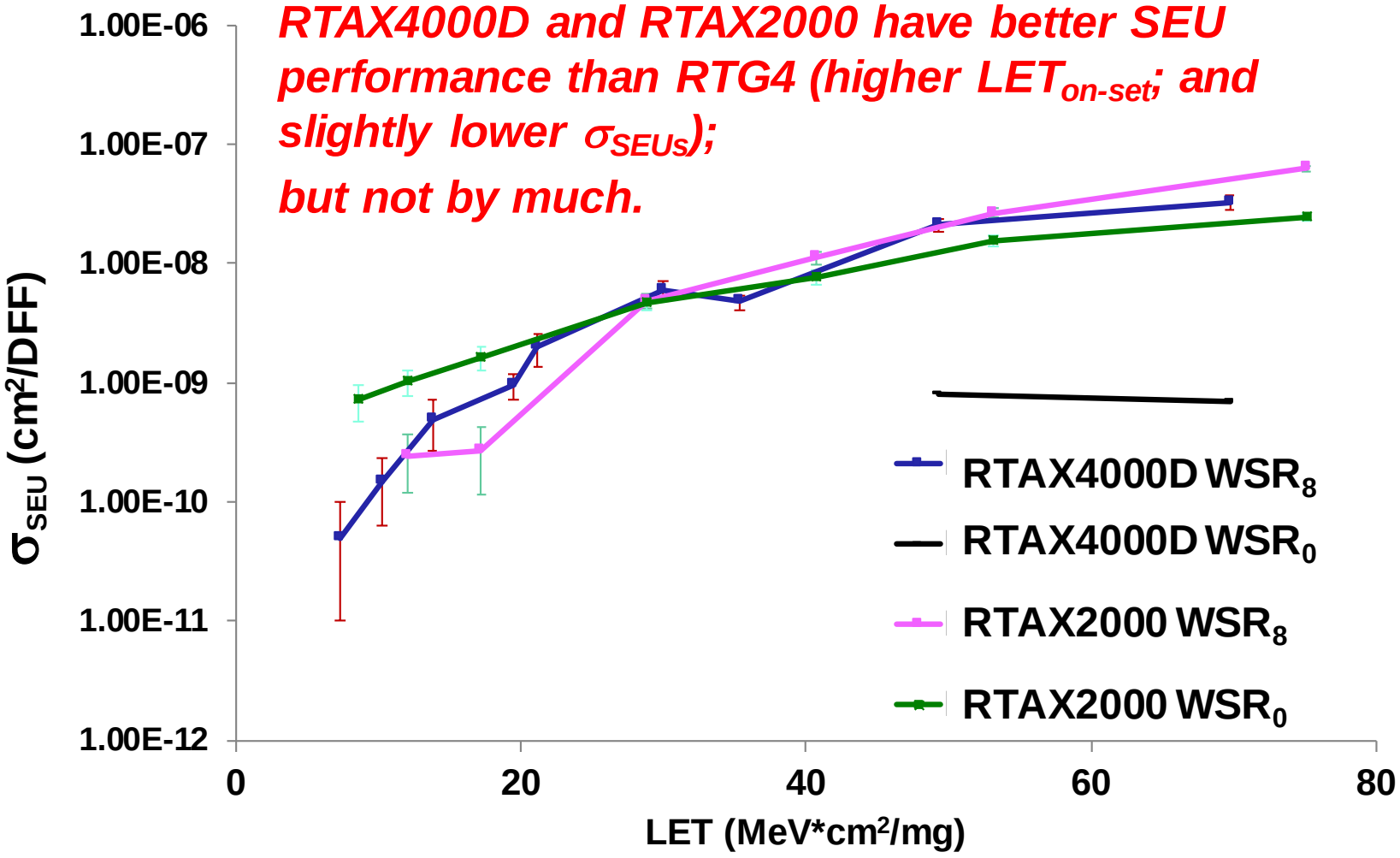
Rev C: WSRs with SET FILTER versus LET at 100MHz



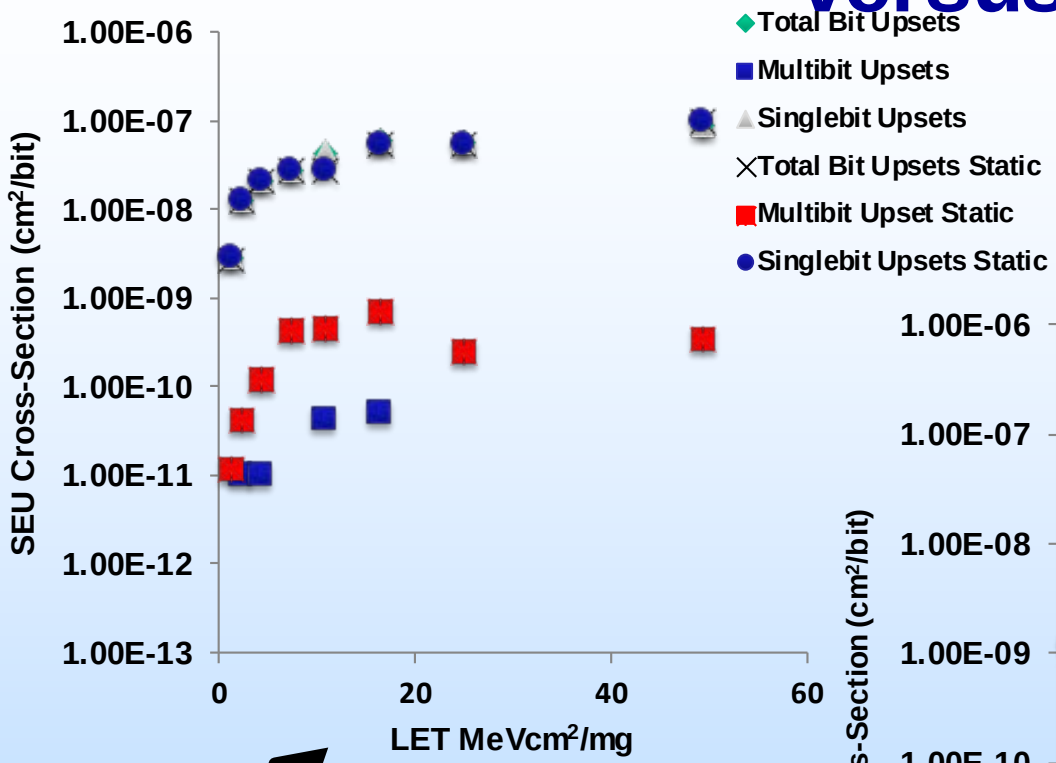
WSR and Counter Accelerated Radiation Test Data Observations

- WSR chains showed a variety of dependencies (all are as expected results for well-mitigated FPGA devices):
  - Increase clock frequency– increase failures.
  - Increase combinatorial logic – increase failures.
  - Increase data change rate – increase failures.
  - Use of flip-flop SET filter – decrease failures.
  - Use of flip-flop SET filter – decreases system operation speed.
- As LET increases, the effectiveness of the SET filter decreases. This is because generated SETs become wider (more energy) and have more power to defeat the SET filter.
- Results (SET filter on) are in-line with the Microsemi SEU radiation hardened predecessor – Microsemi RTAXs family.
- However, the Microsemi RTAXs family had slightly better SEU performance.
  - RTAXs routes had a higher RC component and filtered SETs.
  - RTAXs clock trees were less susceptible.

RTAX4000D and RTAX2000 WSRs at 80MHz with Checkerboard Pattern



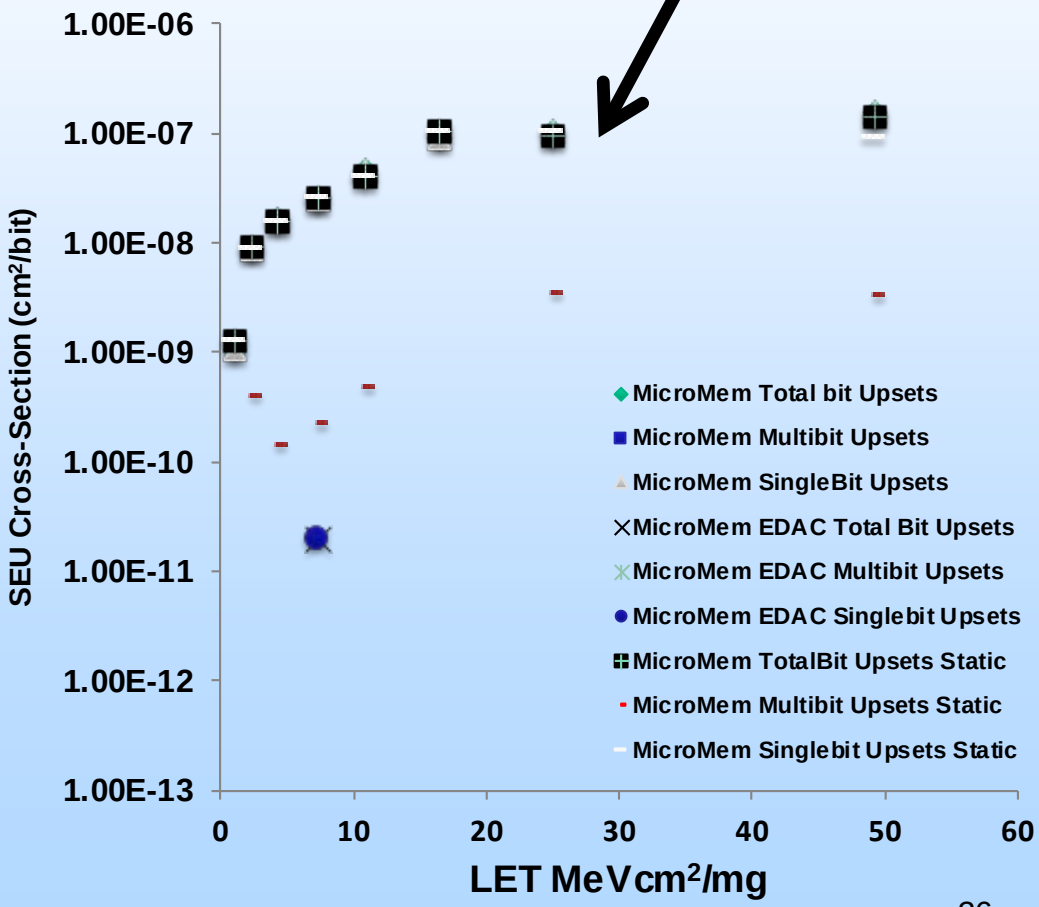
Microsemi SRAM SEU Cross-Sections versus LET



Large SRAM

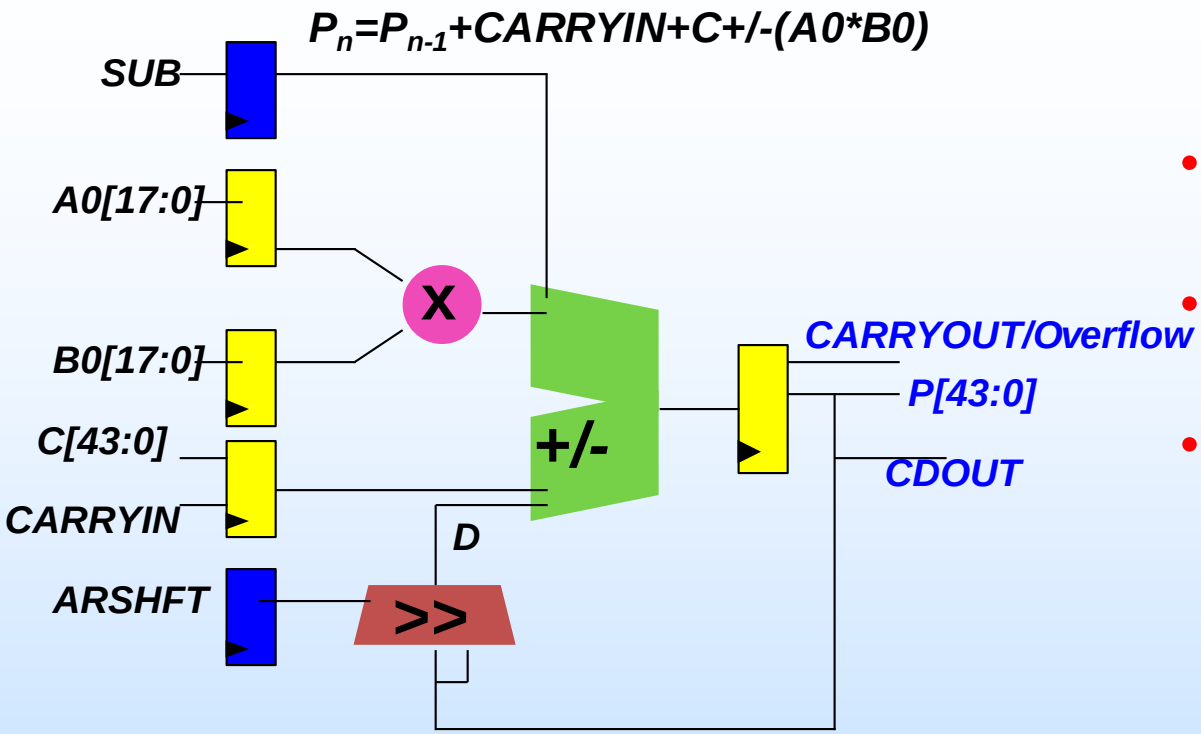
EDAC was only tested with µSRAM

µSRAM

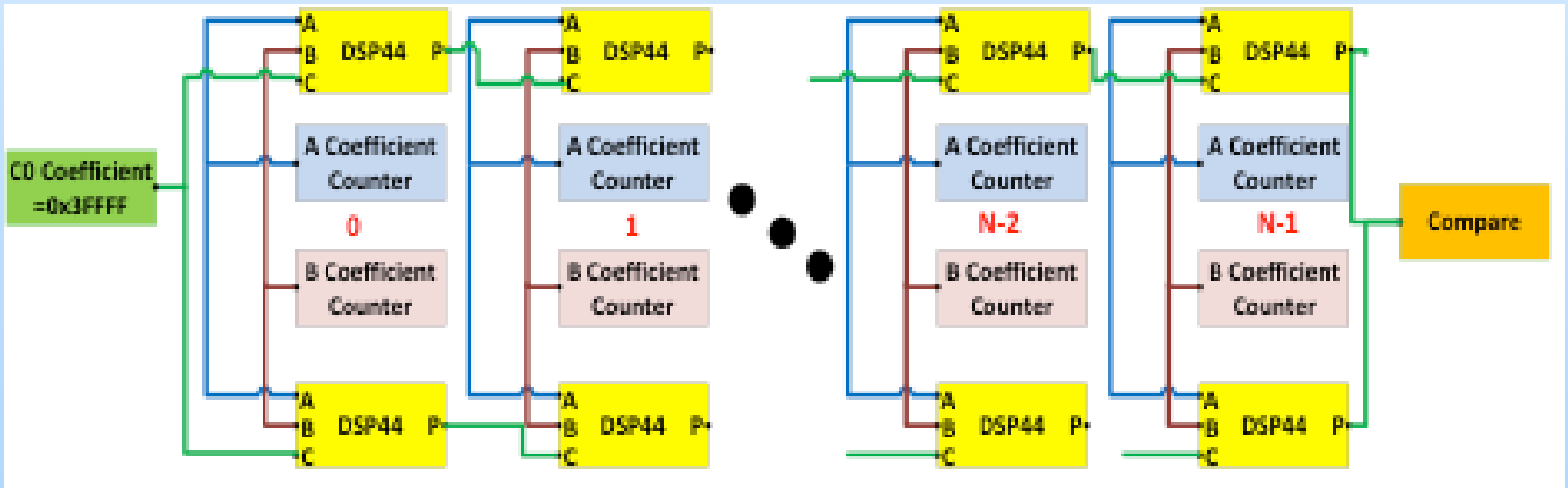


Microsemi included SRAM bit interleaving. Makes a difference with EDAC.

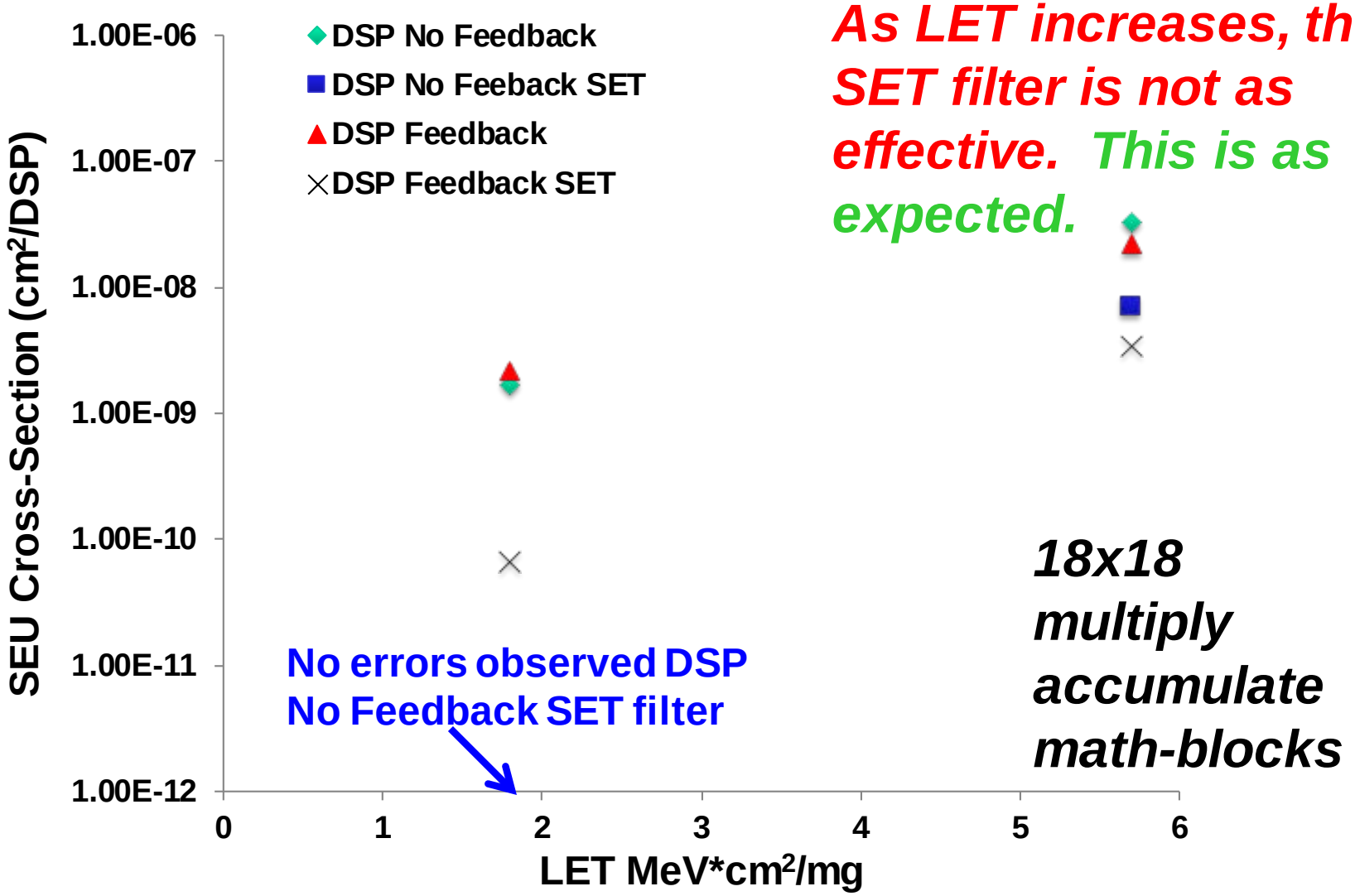
Microsemi Math Block Test Structures



- *18x18 multiply accumulate math-blocks.*
- *Dual redundant chains with a compare.*
- *Coefficients are shared.*



RTG4 Math-block (DSP) SEU Cross-Sections versus LET



As LET increases, the SET filter is not as effective. This is as expected.

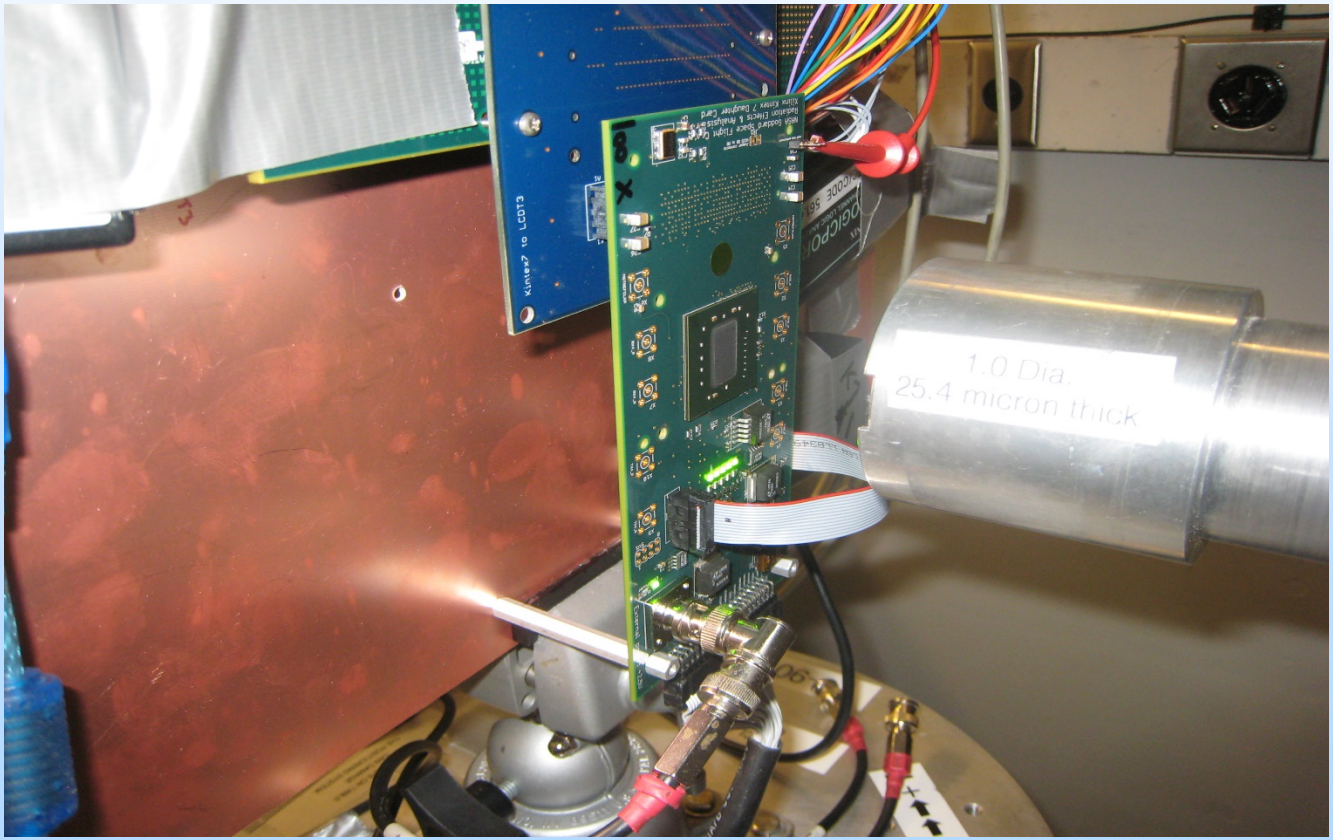
18x18 multiply accumulate math-blocks

Deliverables: Microsemi RTG4 Test Report Submission and Data Summary

- **Two versions of reports have been submitted.**
- **Third version will be completed in June 2017.**
- **As a summary:**
  - **RTG4 is not as SEU hardened as it's predecessor (RTAXs). However, fairly close.**
  - **Exception: embedded SRAM with EDAC – is better in the RTG4.**
  - **Embedded TMR PLL does not operate as expected. No improvement in SEU susceptibility.**
  - **Internal oscillator clock is highly susceptible to SEUs.**
  - **Designs implemented in the RTG4 device do not operate as fast as they do when implemented in the RTG4's predecessor (RTAXs). This is most likely due to the place and route software. However, this is unexpected.**
  - **TBD for NEPP to perform more testing. At this point, additional testing is assumed to be funded by partners or missions.**

SRAM-based FPGA Mitigation Study using Xilinx Kintex-Ultrascale (XCKU040-1LFFVA1156I)

(1) Single event latch-up (SEL)



Impact to Community Kintex-UltraScale

σ_{SEU}: SEU Cross-section *IP: intellectual property*

- **Next generation of FPGA devices following the commercial Xilinx-7 series.**
- **I/O interfaces are significantly more robust.**
- **There are no embedded mitigation circuits in the user fabric. However, higher gate-count better allows the user to insert mitigation into the design.**
- **There is no embedded processor. However, the user can embed a soft-core.**

$$P(fs)_{system} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Design σ_{SEU} *Configuration σ_{SEU}* *Functional logic σ_{SEU}* *SEFI σ_{SEU}*

NEPP performs an independent study to determine the level of SEU susceptibility for the various FPGA components.

Xilinx Kintex-Ultrascale

- **New Entry into the Aerospace Market with COTS Expectation … 20 nm planar process (TSMC).**

Data Transfer Is Key for Our New System Applications: UltraScale Transceivers

	Kintex-Ultrascale		Virtex UltraScale	
Type	GTH	GTY	GTH	GTY
Quantity	16-64	0-32	20-60	0-60
Maximum Data Rate	16.3Gb/s	16.3Gb/s	16.3Gb/s	30.5Gb/s
Minimum Data Rate	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s
Key Applications	Backplane PCIe Gen4 HMC	Backplane PCIe Gen4 HMC	Backplane PCIe Gen4 HMC	100G+Optics Chip-to-Chip 25G+ Backplane HMC

Xilinx Kintex-UltraScale Study Objectives

- **This is an independent investigation that evaluates the single event destructive and transient susceptibility of the the Xilinx Kintex-UltraScale device.**
- **Design/Device susceptibility is determined by monitoring the DUT for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing the DUT to a heavy ion beam.**
- **Potential Single Event Latch-up (SEL) is checked throughout heavy-ion testing by monitoring device current.**
- **This device does not have embedded mitigation. Hence, user implemented mitigation is investigated using Synopsys mitigation tools.**
- **FPGA part# XCKU040-1LFFVA1156I.**
- **Collaboration: Xilinx and Synopsys.**

Beam time was limited: SEL, configuration, and Mitigation.

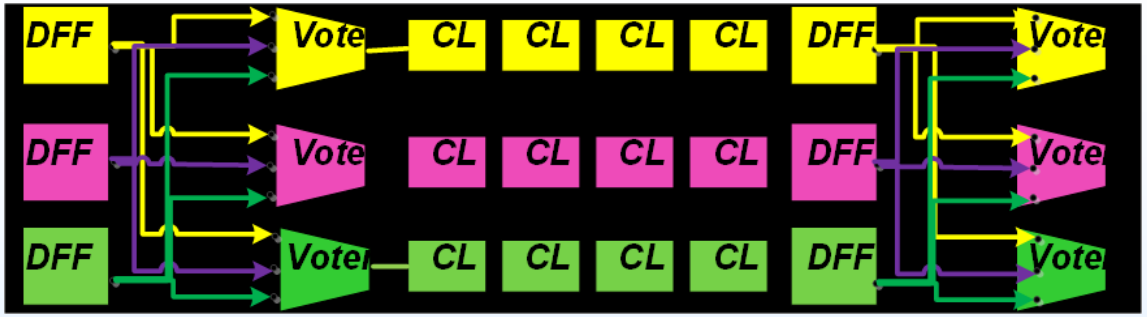
TMR Descriptions

DFF: Edge triggered flip-flop; *CL: Combinatorial Logic*

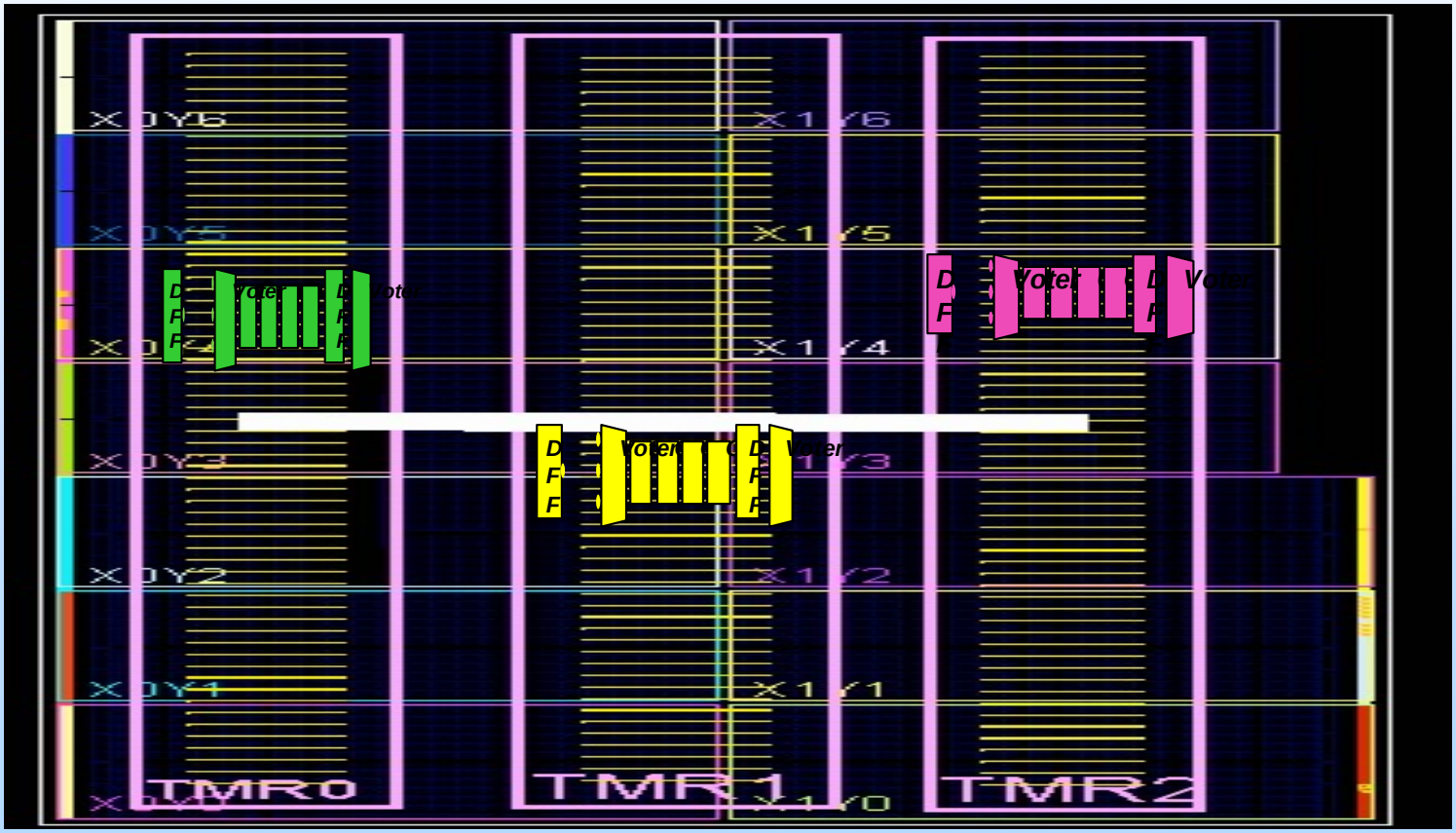
TMR Nomenclature	Description	TMR Acronym
Block TMR	Entire design is triplicated. Voters are placed at the outputs.	BTMR
Local TMR	Only the DFFs are triplicated. Voters are placed after the DFFs.	LTMR
Distributed TMR	DFFs and CL-data-paths are triplicated. Similar to a design being triplicated but voters are placed after the DFFs.	DTMR
Global TMR	DFFs, CL-data-paths and global routes are triplicated. Voters are placed after the DFFs.	GTMR or XTMR

Note: It has been suggested to separate (partition) TMR domains in SRAM based designs so that there are no overlapped shared resources. Shared resources become single points of failure.

DTMR Partitioning



SEUs that occur in one TMR domain are expected to be mitigated.



Kintex-Ultrascale Designs Tested

Test Structure	Frequency Range
Counter Array No TMR	50MHz
Counter Array DTMR with partitioning	50MHz
Counter Array DTMR no partitioning	50MHz
Counter Array BTMR with partition	50MHz
Counter Array LTMR with partition	50MHz

NEPP has the only current heavy-ion data for the Synopsys mitigation tool.

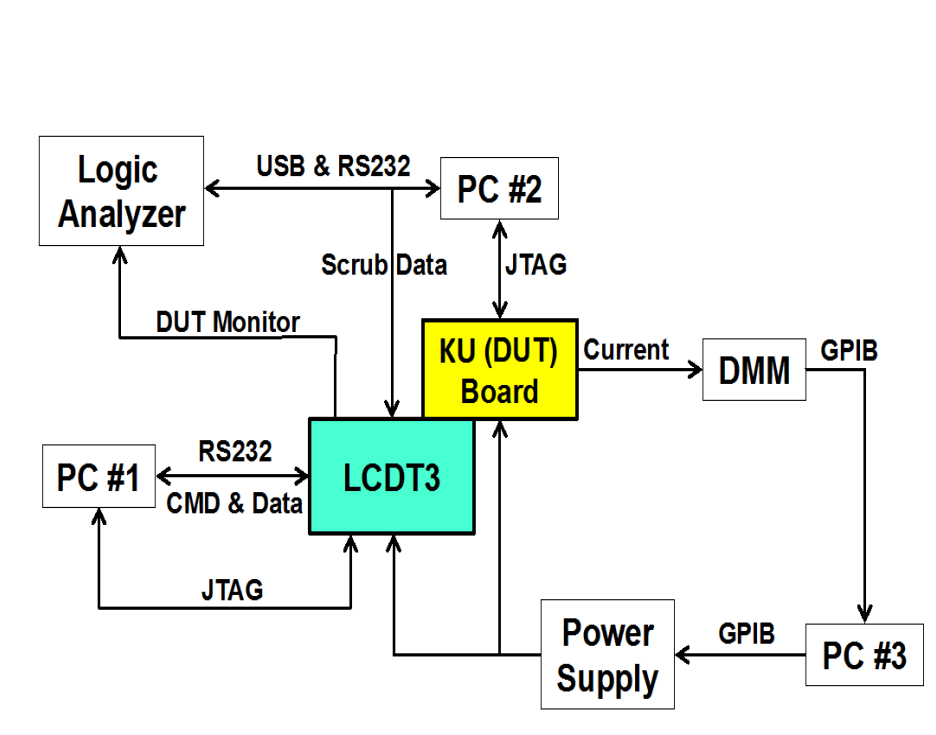
Test Facility Conditions

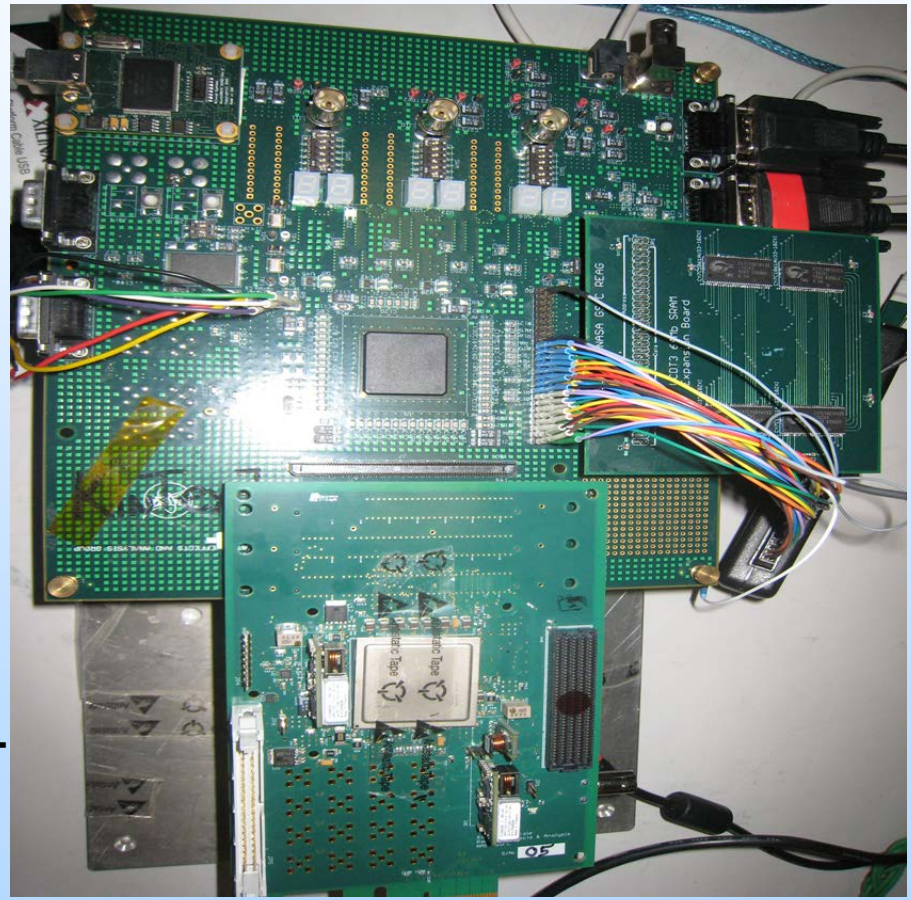
- Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 25 MeV/amu tune).
- Flux: 1×10^2 to 5×10^5 particles/cm^2·s
- Fluence: All tests were run to 1×10^7 particles/cm^2 or until destructive or functional events occurred.
- Test temperature: Room temperature

Ion	Energy (MEV/Nucleon)	LET (MeV*cm^2/mg) 0°	LET (MeV*cm^2/mg) 60 °
He	25	.07	.14
N	25	.9	.18
Ne	25	1.8	3.6
Ar	25	5.5	11.0
Kr	25	19.8	40.0
Xe**	25	38.9	78.8

We were unable to obtain Xe during our testing

Kintex-UltraScale DUT And Tester



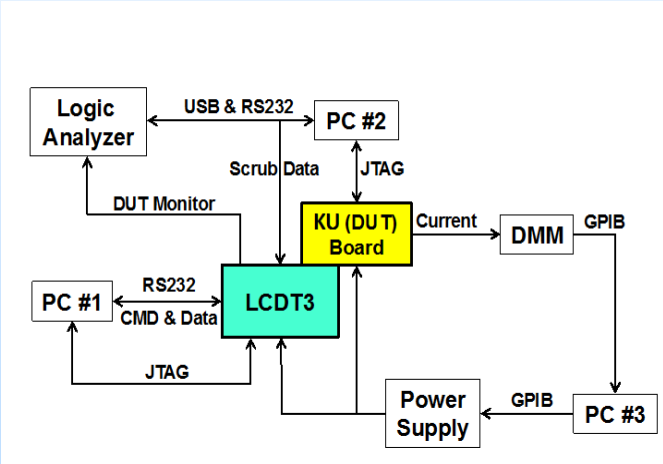


DMM (digital multimeter):

- Scan Kintex-UltraScale supply current measurement.
- VCCINT, VCCO, VCCAUX, VCCMGT , VTxRx.
- Monitors temperature from the on-chip diode.

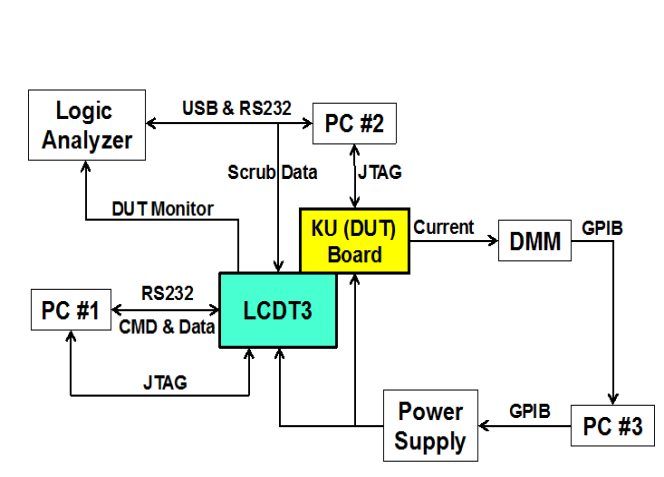
Test Setup - For Your Future Reference (1)

- **LCDT3**
  - Control Kintex-UltraScale Operation Modes and Execution.
  - Collect All Data from Kintex-UltraScale Board, analyze data and Report the results to PC #1.
- **PC #1**
  - Configure LCDT3 via JTAG. Send Commands LCDT via RS232. Receive Data from LCDT via RS232.
- **PC #2**
  - Configure Kintex-UltraScale via JTAG. Readback Kintex-UltraScale configuration data after irradiation.
  - Send Kintex-UltraScale configuration data for DUT configuration scrubbing via USB & RS232.
  - Run and display logic analyzer capture via USB.



Test Setup - For Your Future Reference (2)

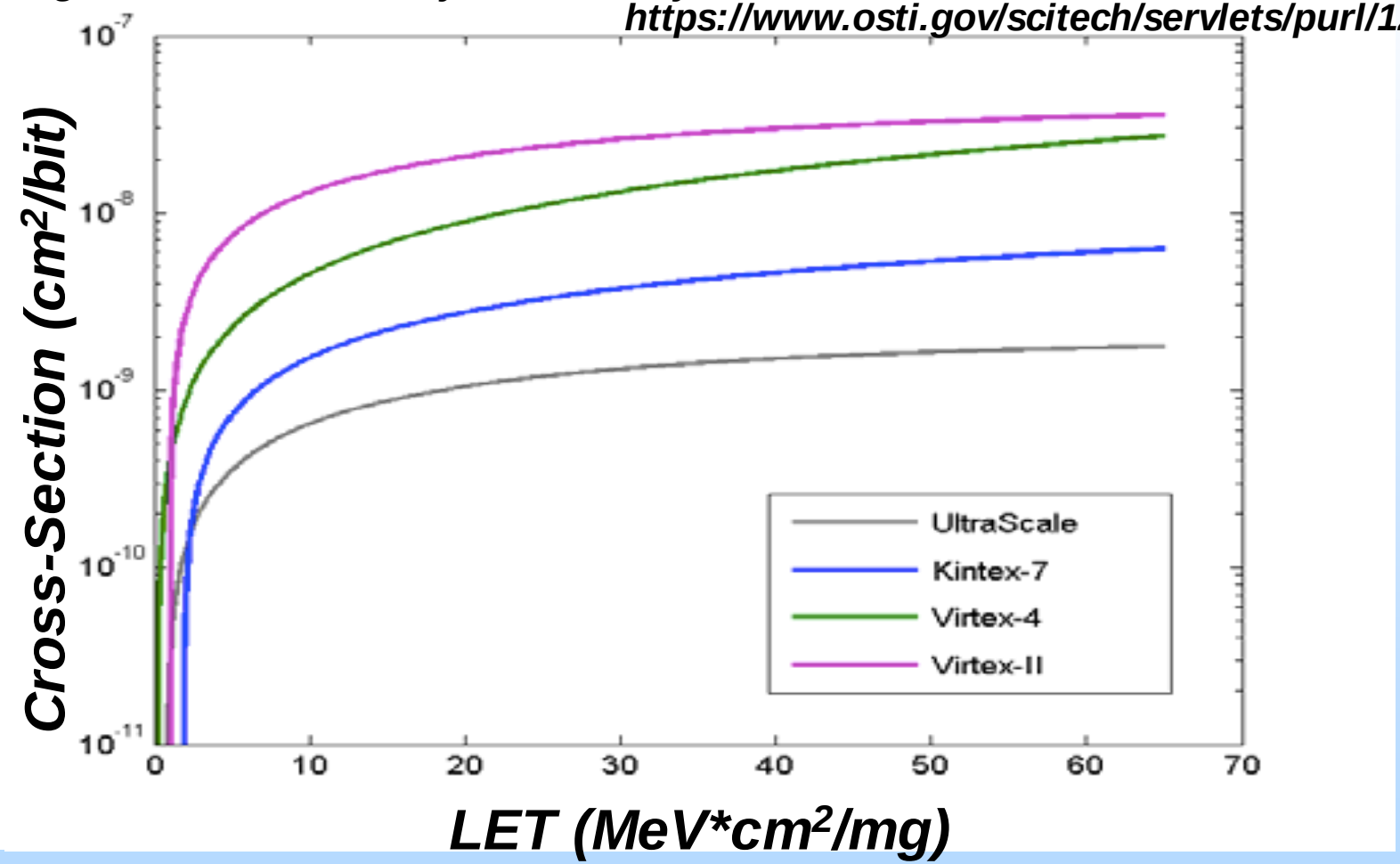
- PC #3
  - Control DC Power Supply via GPIB.
  - Collect current readings from DMM via GPIB.
- Logic Analyzer
  - Monitor Kintex-UltraScale operation status.
- Power Supply
  - Provide power to both LCDT3 & Kintex-UltraScale board.
- DMM (digital multimeter)
  - Scan Kintex-UltraScale supply current measurement.
  - VCCINT, VCCO, VCCAUX, VCCMGT , VTxRx.
  - Monitors temperature from the on-chip diode.
- Kintex-UltraScale DUT
  - Although there are various components on this board (as illustrated in Figure 4), only the mounted Kintex-UltraScale device is subjected to the heavy-ion beam



Xilinx Scaling Family Trends for Configuration Bits in Heavy Ions

David Lee et. al. "Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation"

https://www.osti.gov/scitech/servlets/purl/1263983



Daily upsets in configuration in LEO and GEO are expected.

BRAM Interconnects

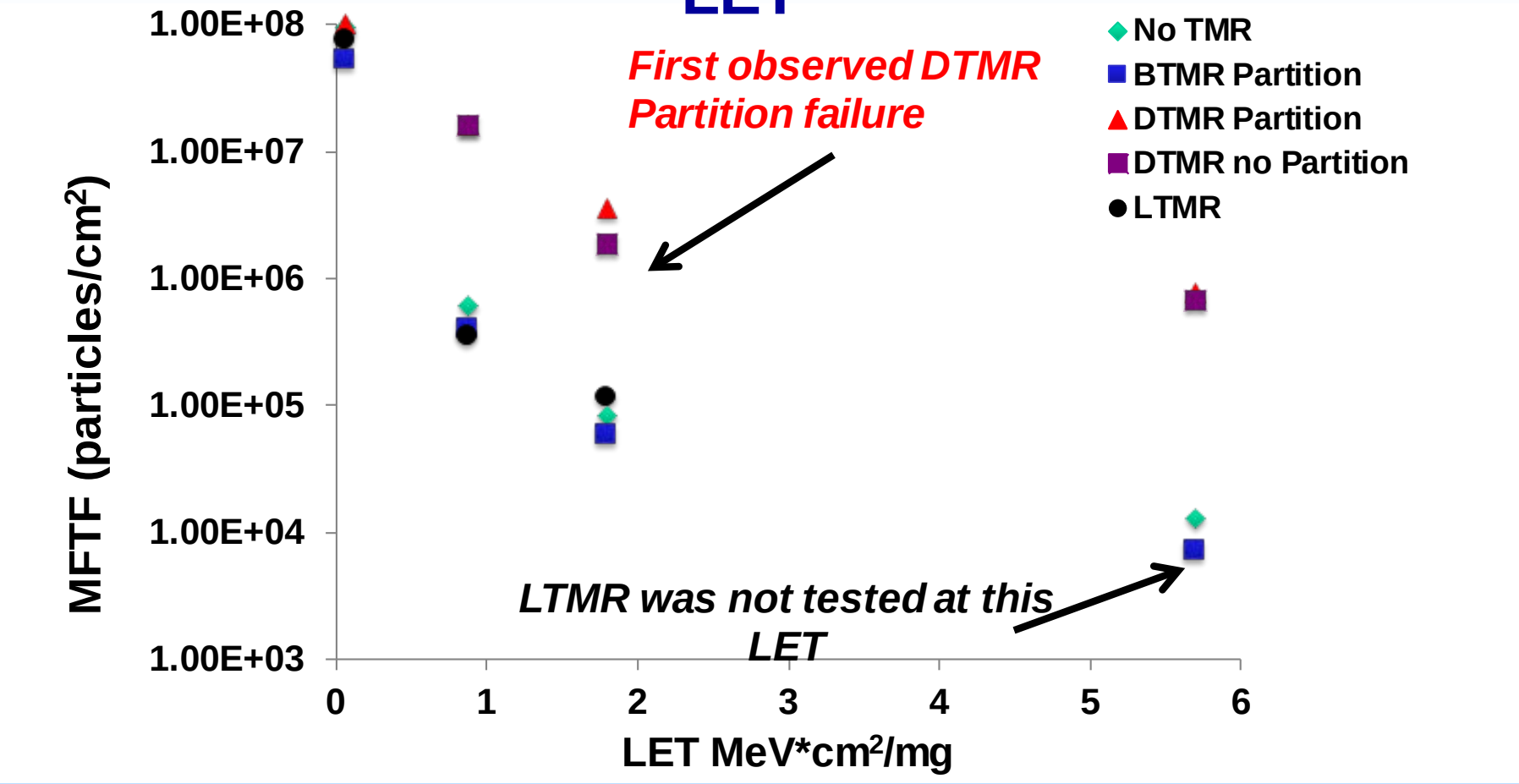
- In the design bit-stream, BRAM interconnects are sprinkled within the BRAM data area.
- No interconnect upsets observed with LET lower than 0.87 MeVcm^2/mg.
  - The is mostly likely a statistical numbers issue. The number of SEUs that occur below 0.87 MeVcm^2/mg is significantly small.
- Starting at LET = 0.87 MeVcm^2 , multiple bit BRAM interconnects SEUs were observed.
  - Number of upsets is a power of two and upsets are not in the same memory word.
  - This result illustrates the memory interleaving that Xilinx implemented.
  - This result also illustrates that a single event more than likely affected multiple interconnects.
- Additional testing needs to be performed to get BRAM data SEU cross-sections and error responses.

History of Xilinx and Single Event Latchup (SEL) or Latchup-Like Events: Virtex 2 through UltraScale Series

Latchup-like event: A component is affected by an ionizing particle such that current is increased and held. A power-cycle is required for the circuit to release the current.

- **Xilinx Virtex 2: Latchup-like events have been observed in flight. Most likely due to embedded half-latches in the device.**
- **Xilinx Virtex 5: Half-latches were removed. No latchup-like events observed during SEE testing or in flight.**
- **Xilinx 7-series: Is it SEL or latchup-like? Observed only on 7-series devices that contained 3.3V I/O. Devices that do not contain such I/O have no latchup-like events.**
- **Xilinx UltraScale series no latchup-like event observed.**

Kintex-UltraScale Mitigation Study: Counter Arrays Mean Fluence to Failure (MFTF) versus LET

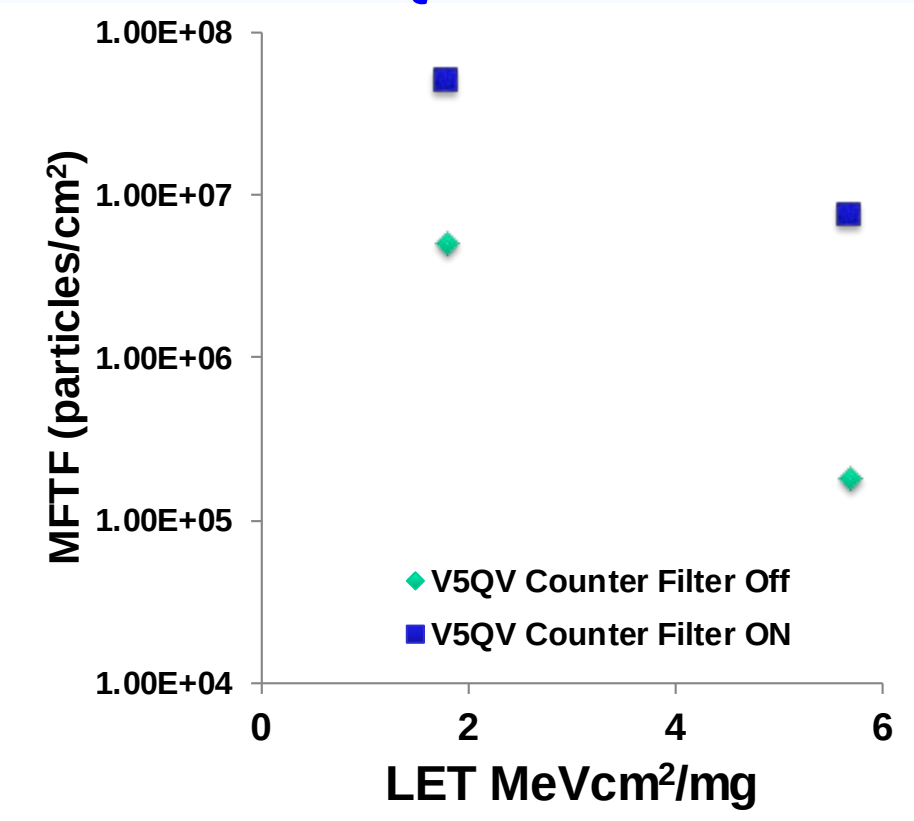


Kintex-UltraScale Data drops off quicker than radiation hardened Xilinx Virtex (V5QV).

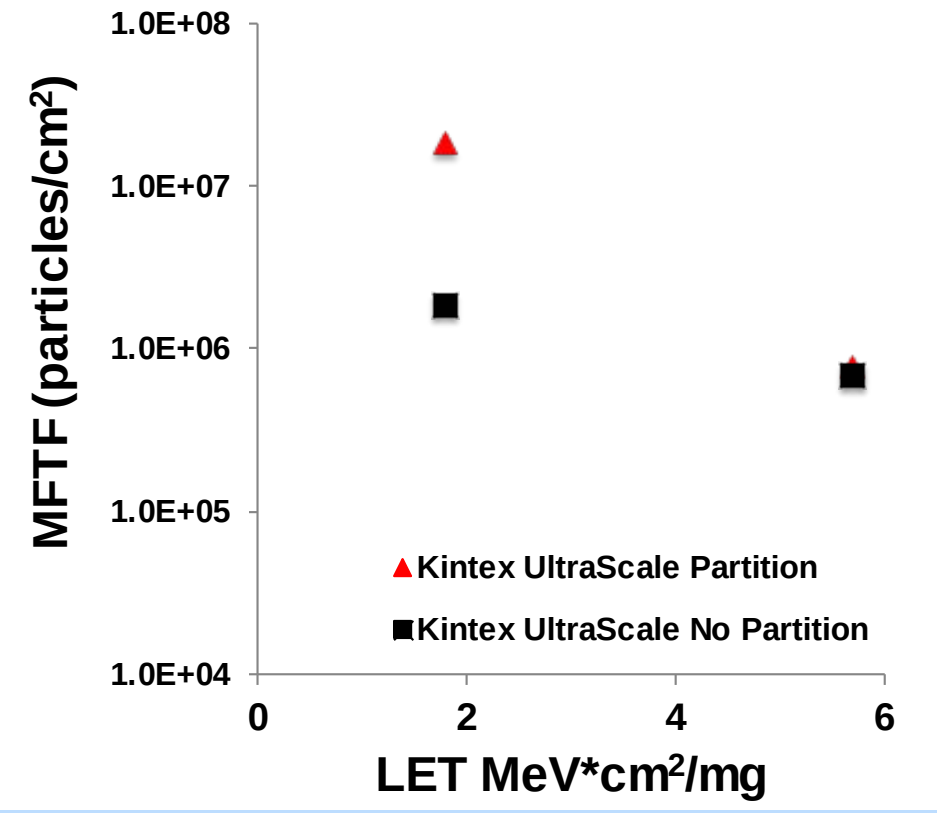
More SEU testing should be performed for more detailed comparisons.

Comparison of V5QV and Kintex UltraScale with Mitigation

V5QV Counters



Kintex UltraScale DTMR Counters



Synopsys results are looking good.

Summary of Mitigation Application to Kintex-UltraScale during SEU-Heavy-Ion Testing

SEFI: single event functional interrupt

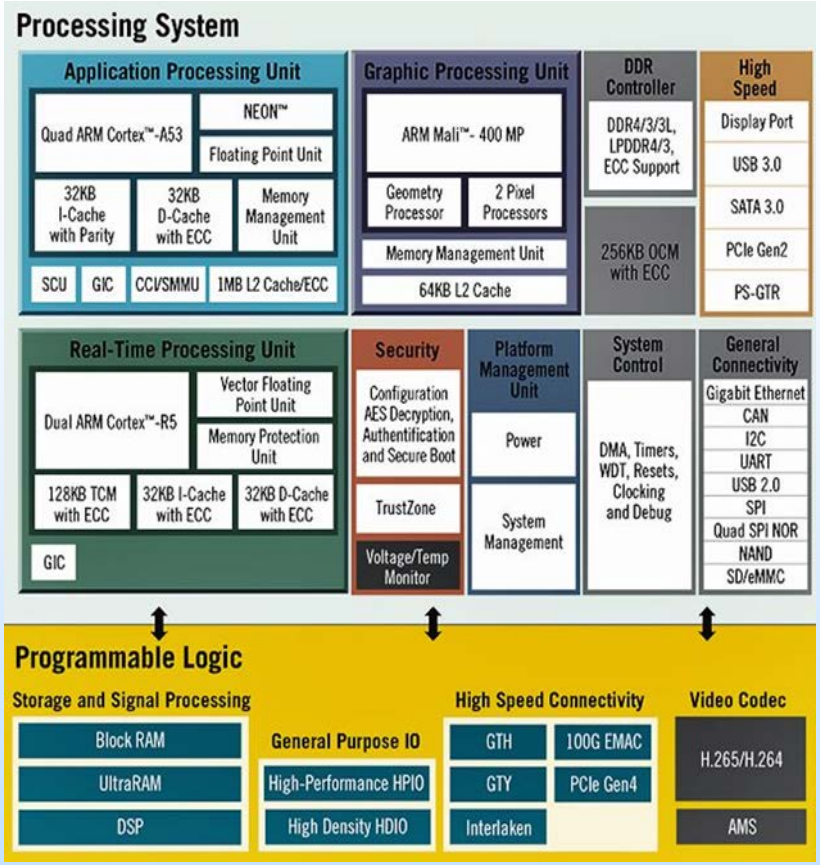
- Mitigation study proves DTMR is the strongest mitigation scheme implemented in an SRAM-based FPGA.
  - However, for flushable designs BTMR might be acceptable.
  - LTMR is not acceptable in SRAM-based FPGAs for any design.
  - Partitioning may not be necessary.
- Although GTMR has been implemented in V5 families and earlier Xilinx device families, NEPP has suggested to avoid GTMR because clock skew is difficult to control.
  - In 2015-2016, via heavy-ion SEU testing, It has been observed in the Xilinx 7-series, that race conditions due to clock skew are unavoidable.
  - This is due to the speed of combinatorial logic and route delays in the 7-series versus earlier Xilinx FPGA device families.
- Synopsis tool has improved for simple designs. They are still working on IP core instantiations and other challenges.
- Mitigation and IP cores are still a major concern!!!!!!!!!!!!!

Deliverables: Xilinx Kintex-UltraScale Test Report Submission and Data Summary Test Report

- **The full Kintex-UltraScale SEU dataset is still currently being analyzed and will be available by June 2017.**

- **As a summary:**
  - **NEPP has provided insight into Xilinx potential latchup-like events.**
  - **Through previous heavy-ion studies and design experience, NEPP has provided Synopsys information for sufficient mitigation strategies per FPGA type.**
  - **TBD for NEPP to perform more testing. At this point, additional testing is assumed to be funded by partners or missions.**

Xilinx Zynq UltraScale+



SRAM based Configuration. No radiation hardening is applied to flip-flops. However, manufacturer hopes FinFET technology will reduce SEU susceptibility.

- **New Entry into the Aerospace Market with COTS Expectation.**
  - **16nm FinFet vertical process (TSMC).**
  - **Depending on mission requirements, additional mitigation may be required.**
- **Zync UltraScale+ Includes:**
  - **Dual and quad core variants of the ARM Cortex-A53 (APU).**
  - **Dual-core ARM Cortex-R5 (RPU).**
  - **Dedicated ARM graphics processing unit (GPU).**

Xilinx Kintex-Ultrascale+ Transceivers

Data Transfer Is Key for Our New System Applications: UltraScale+ Transceivers

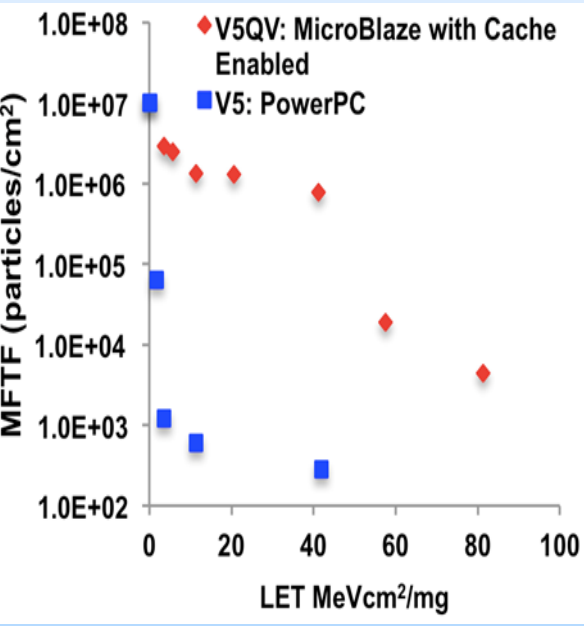
	Kintex-Ultrascale+		MPSoC UltraScale+		
Type	GTH	GTY	PS-GTR	GTH	GTY
Quantity	20-60	0-60	4	0-44	0-28
Maximum Data Rate	16.3Gb/s	32.75Gb/s	6.0Gb/s	16.3Gb/s	32.75Gb/s
Minimum Data Rate	0.5Gb/s	0.5Gb/s	1.25Gb/s	0.5Gb/s	0.5Gb/s
Key Applications	Backplane PCIe Gen4 HMC	100G+Optics Chip-to-Chip 25G+ Backplane HMC	PCIe Gen2 USB Ethernet	Backplane PCIe Gen4 HMC	100G+Optics Chip-to-Chip 25G+ Backplane HMC

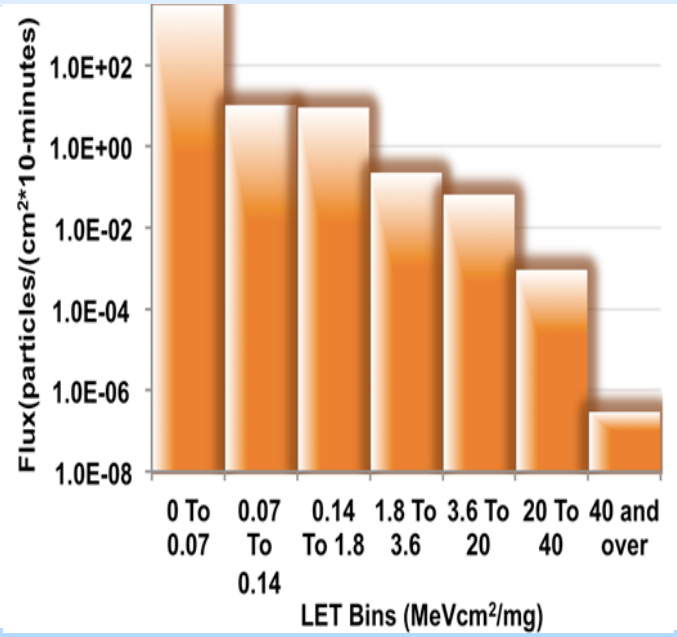
Xilinx UltraScale+ Schedule

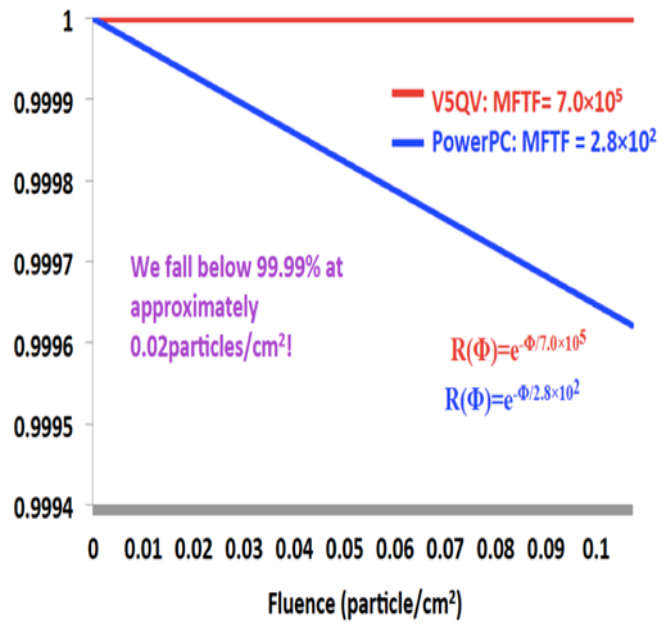
- We plan to test two platforms:
  - MPSoC evaluation board.
  - Custom Kintex-Ultrascale+ daughter card. Designed by NEPP.
- We currently have one evaluation board. MPSoC evaluation boards (ready for testing) will be in hand in June 2017.
- Proton testing using the MPSoC evaluation board is planned for August 2017 timeframe.
- Custom board is planned to be completed October 2017.
- Heavy ion testing will occur FY17 and FY18.
- Current Partners:
  - NASA Goddard Science Data Processing Branch,
  - Sandia National Laboratories,
  - Xilinx,
  - Synopsys,
  - We are looking for additional collaboration.

Development of New Methodology for Characterizing SEU System Response (1)

- This study transforms proven classical reliability models into the SEU particle fluence domain. The intent is to better characterize SEU responses for complex systems.
- Will be discussed in further detail in another ETW presentation.
- Deliverables:
  - Development of analysis (ongoing).
  - Preliminary guidelines documentation submission in FY18.







Mean fluence to failure (MFTF) *Environment data* *Reliability Curve*

Development of New Methodology for Characterizing SEU System Response (2)

- The proposed method does not rely on data-fitting and hence removes a significant source of error.
- The proposed method provides information for highly SEU-susceptible scenarios; hence enabling a better choice of mitigation strategy.
- This methodology expresses SEU behavior and response in terms that missions understand via classical reliability metrics.

- **Presentations:**
  - Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2017 in Reno, NV.
  - Single Event Effects (SEE)/Military Aerospace Programmable Logic Devices (MAPLD) 2017 in San Diego, CA.
  - Submission to IEEE Radiation and its Effects on Components and Systems (RADECS) 2017. Conference will be held in Geneva, SUI.

FPGA Security and Trust

- **Goal: Support U.S. government concerns regarding security and trust in FPGAs. Enhancement to conventional assurance procedures.**
- **2017 Workshop and Conference participation:**
  - **Xilinx Security Working Group (XSWG) 2016 in Longmont, CO.**
  - **Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2017 in Reno, NV.**
  - **Hardened Electronics and Radiation Technology (HEART) 2017 in Denver, CO.**
  - **Hardware-Oriented Security and Trust (HOST) 2017, McLean, VA.**
  - **Joint Federated Assurance Center (JFAC) FPGA working group: Trusted Microelectronics Special Topic: Field Programmable Gate Array Assurance Workshop, McLean, VA.**
- **Collaboration with: Aerospace Corporation, Ball Aerospace, SEAKR, Sandia National Laboratories, Air Force Research Laboratory, Naval Surface Warfare Center – Crane, JFAC, OneSpin, Mentor Graphics, Synopsys, Cadence, and other agencies.**
  - **Meetings, consultations, and presentations.**

Questions?